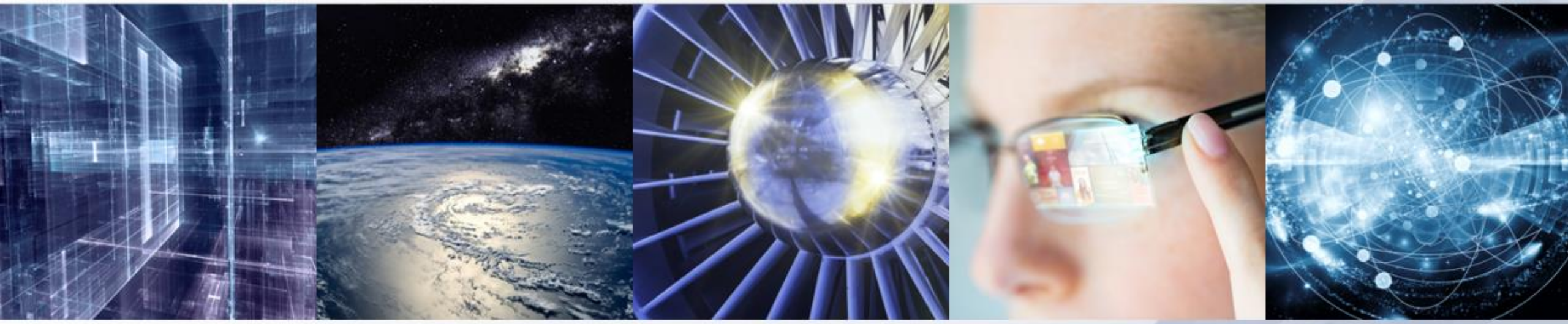

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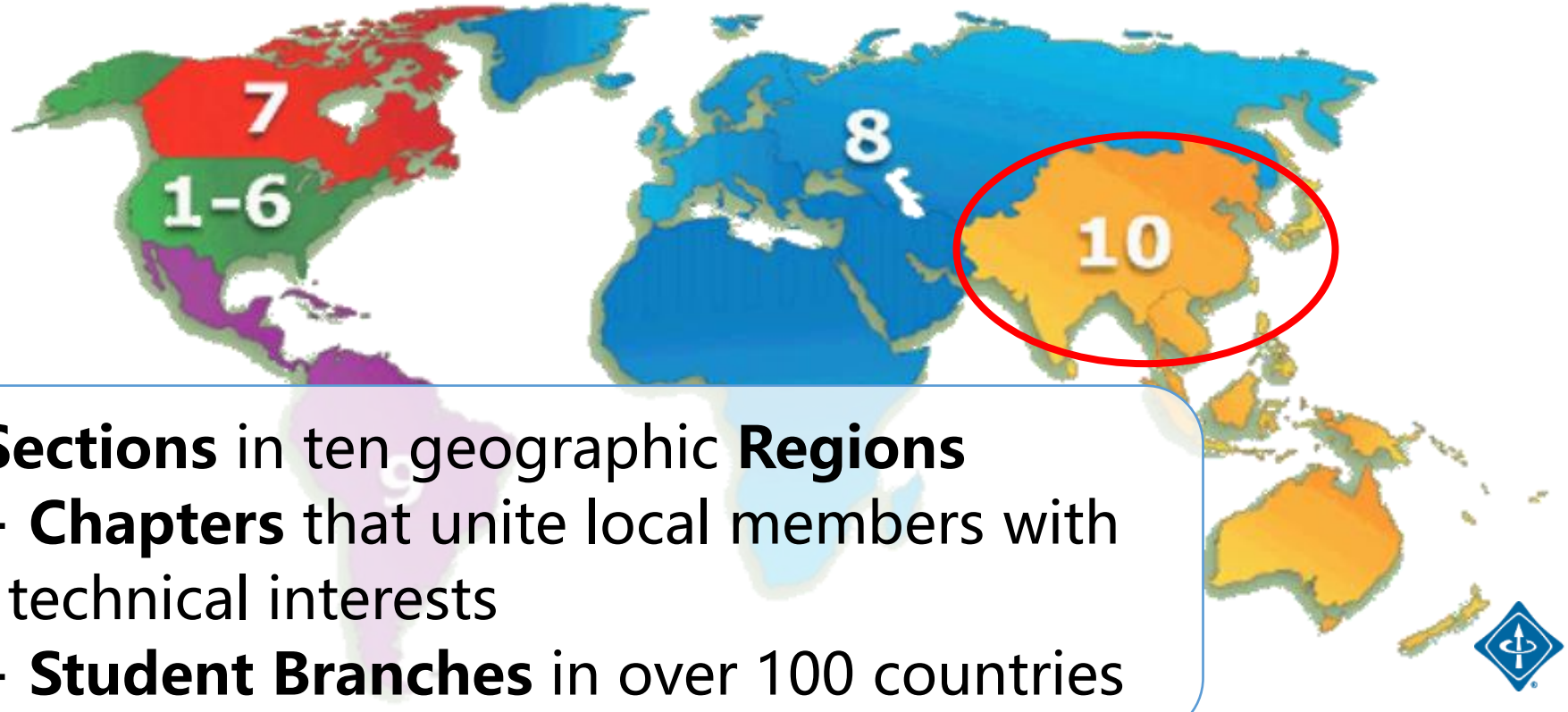

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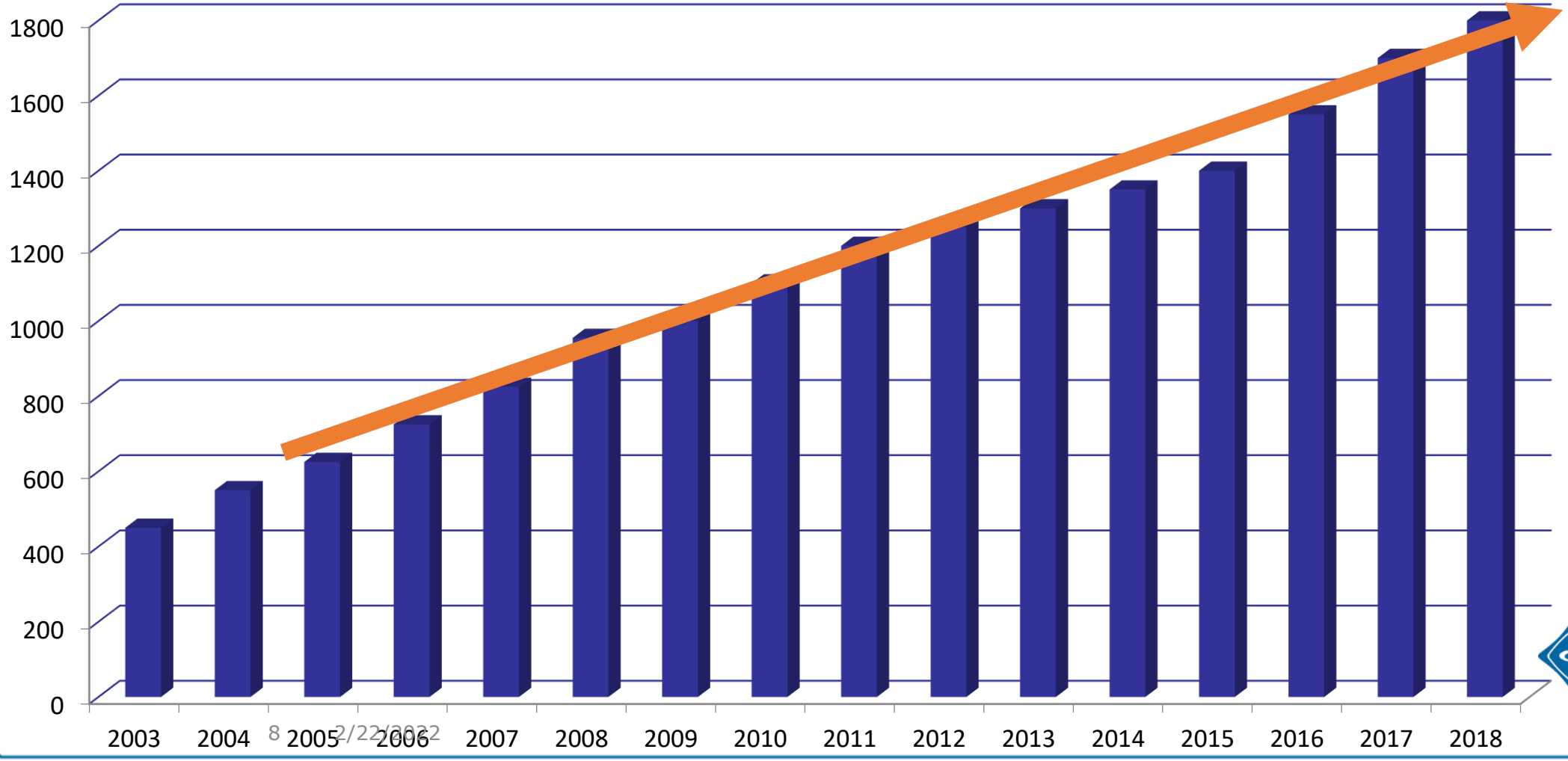

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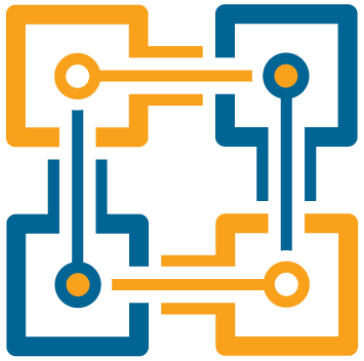

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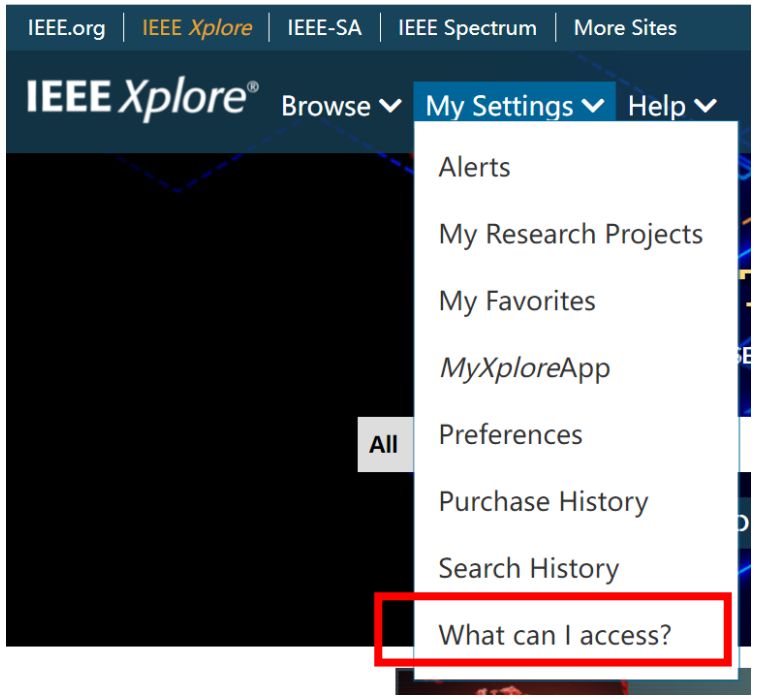

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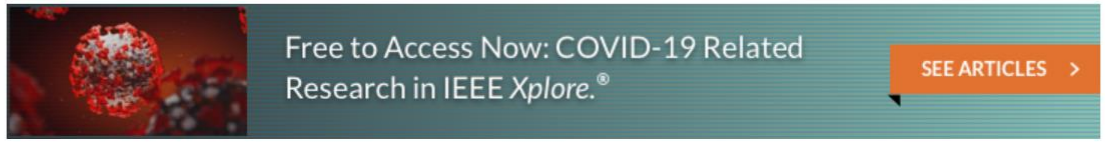

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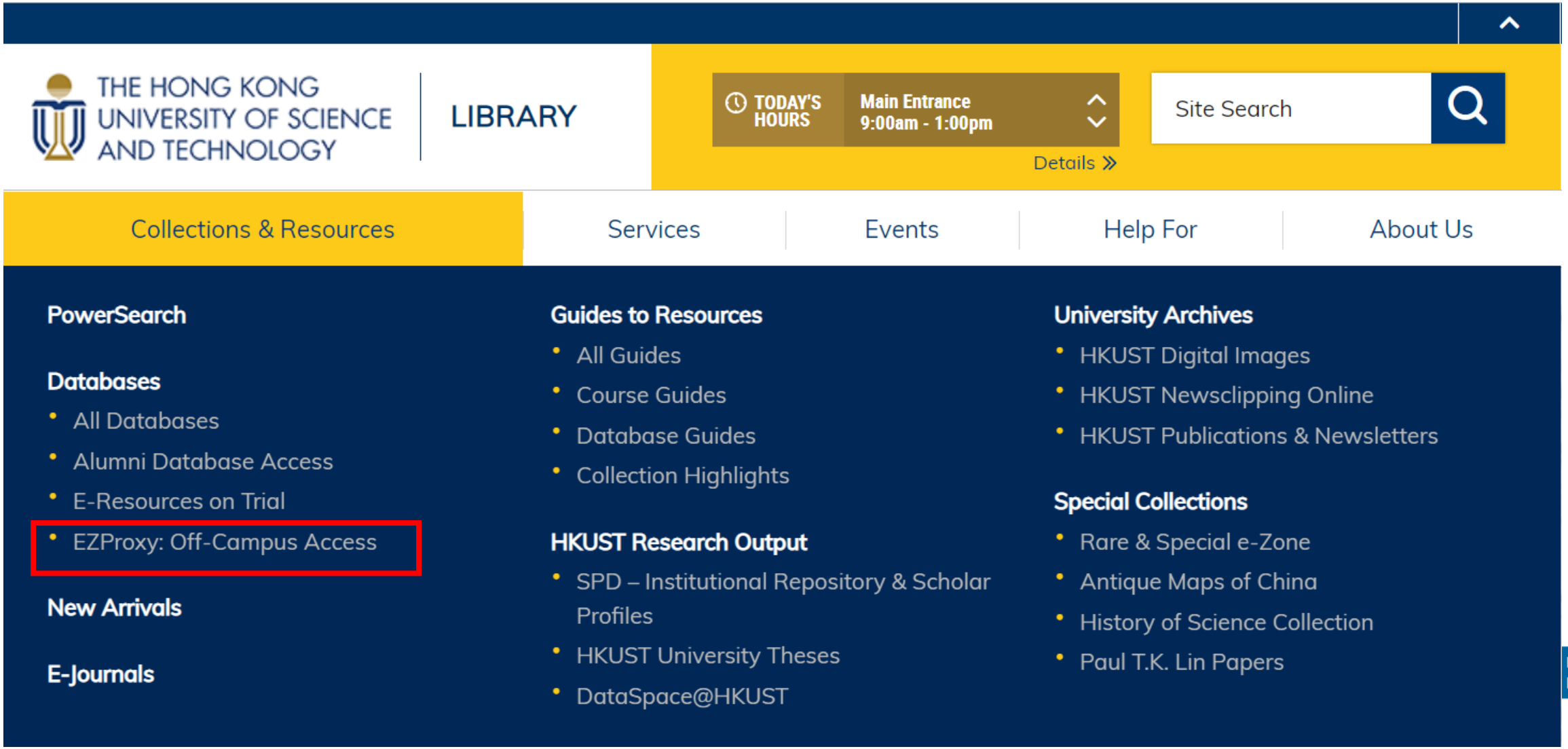

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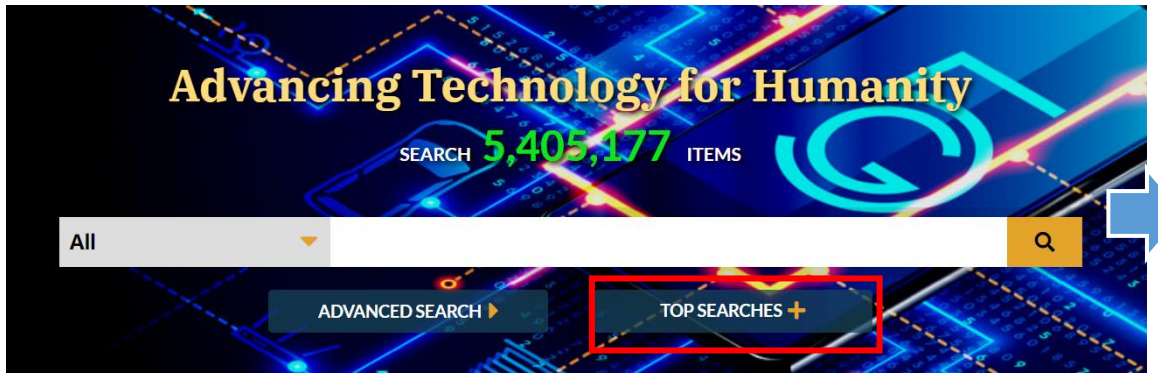

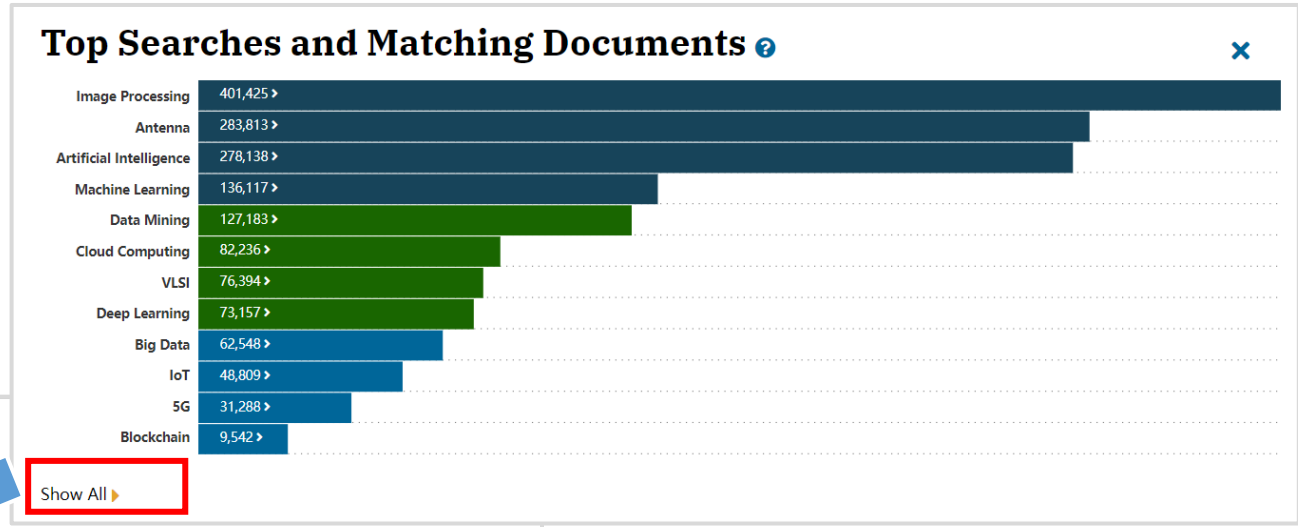

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Biography
Raymond W. Yeung (Fellow, IEEE) was born in Hong Kong in June 1962. He received the B.S., M.Eng., and Ph.D. degrees in electrical engineering from Cornell University, Ithaca, NY, USA, in 1984, 1985, and 1988, respectively.,He was on leave at the École Nationale Supérieure des Télécommunications, Paris, France, in Fall 1986. He was a Member of Technical Staff of AT&T Bell Laboratories from 1988 to 1991. Since 1991, he has been with The Chinese University of Hong Kong, where he is currently a Choh-Ming Li Professor of information engineering and the Co-Director of the Institute of Network Coding. He has held visiting positions at Cornell University, Nankai University, Bielefeld University, the University of Copenhagen, the Tokyo Institute of ... Show More

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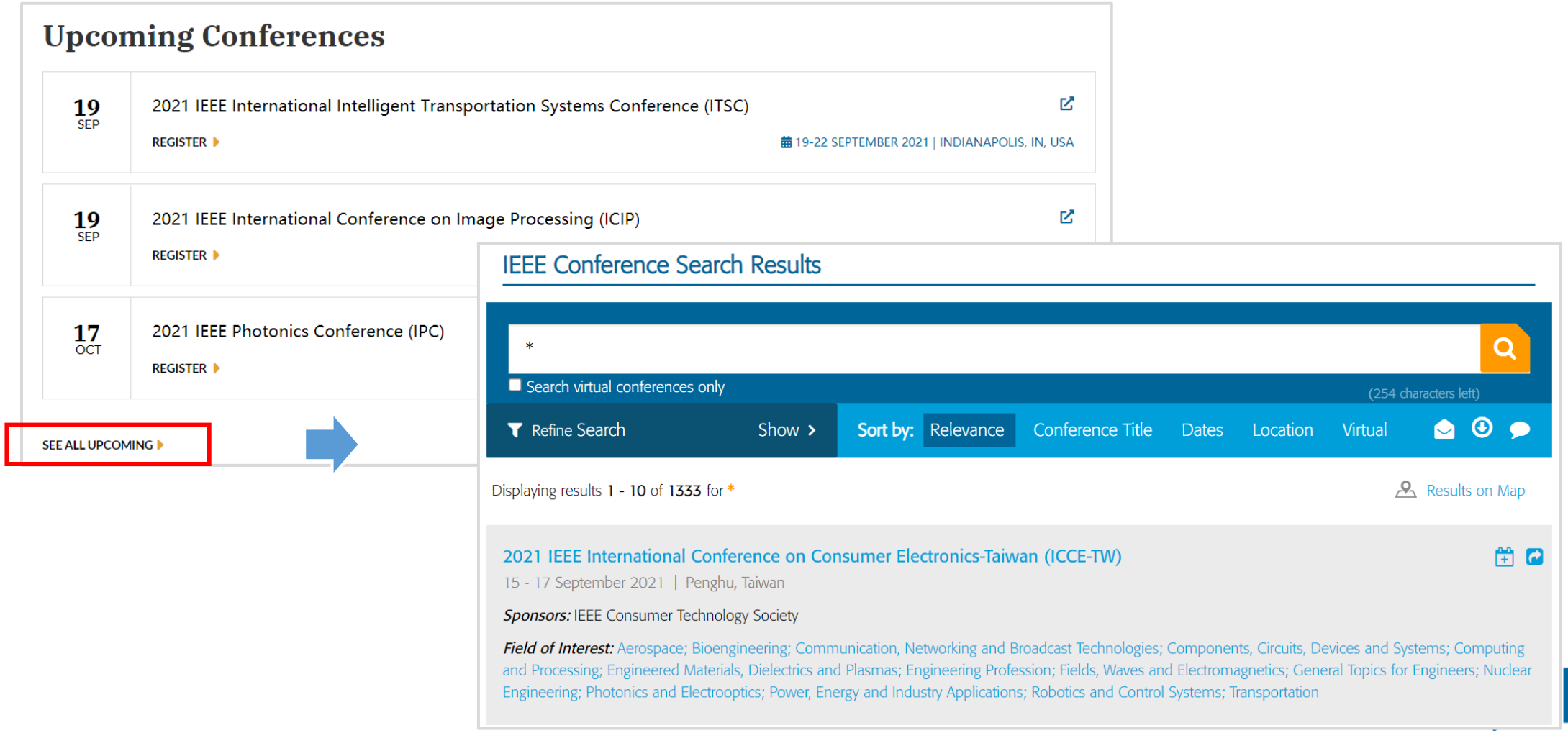

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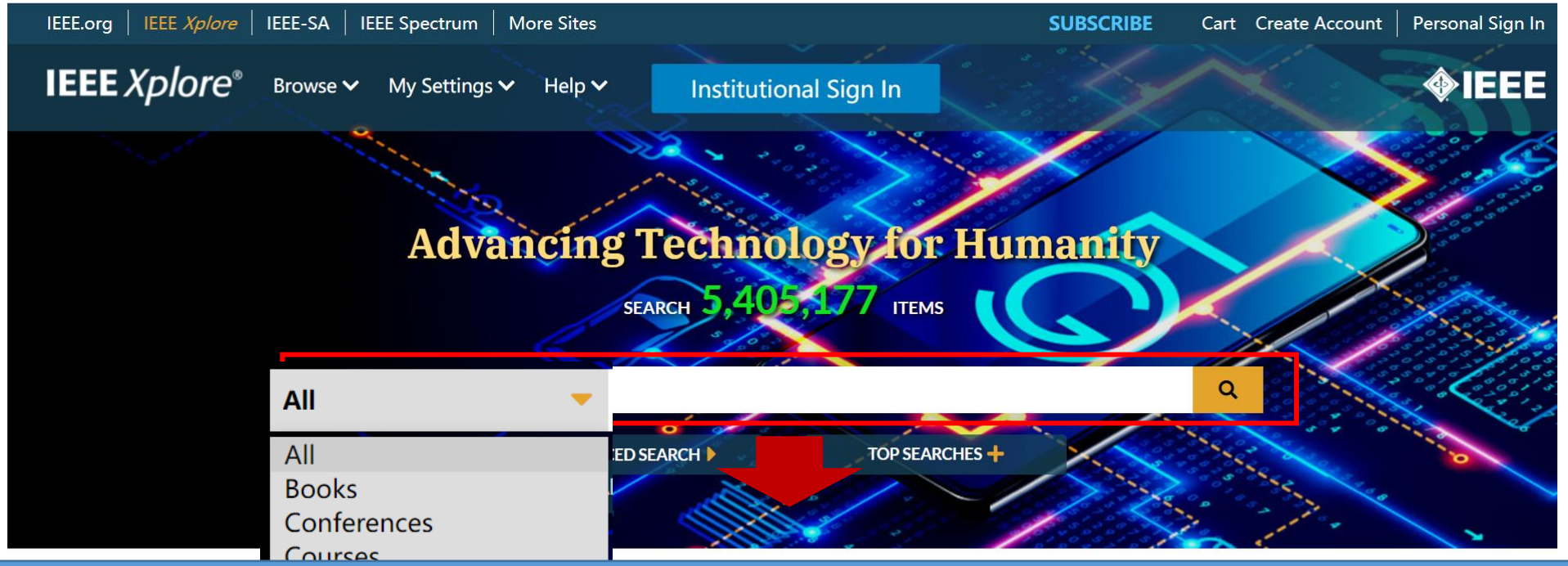

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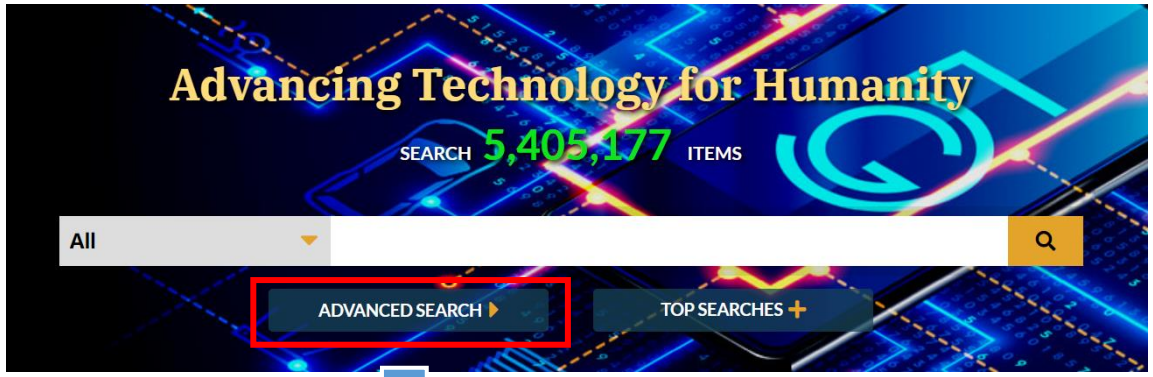

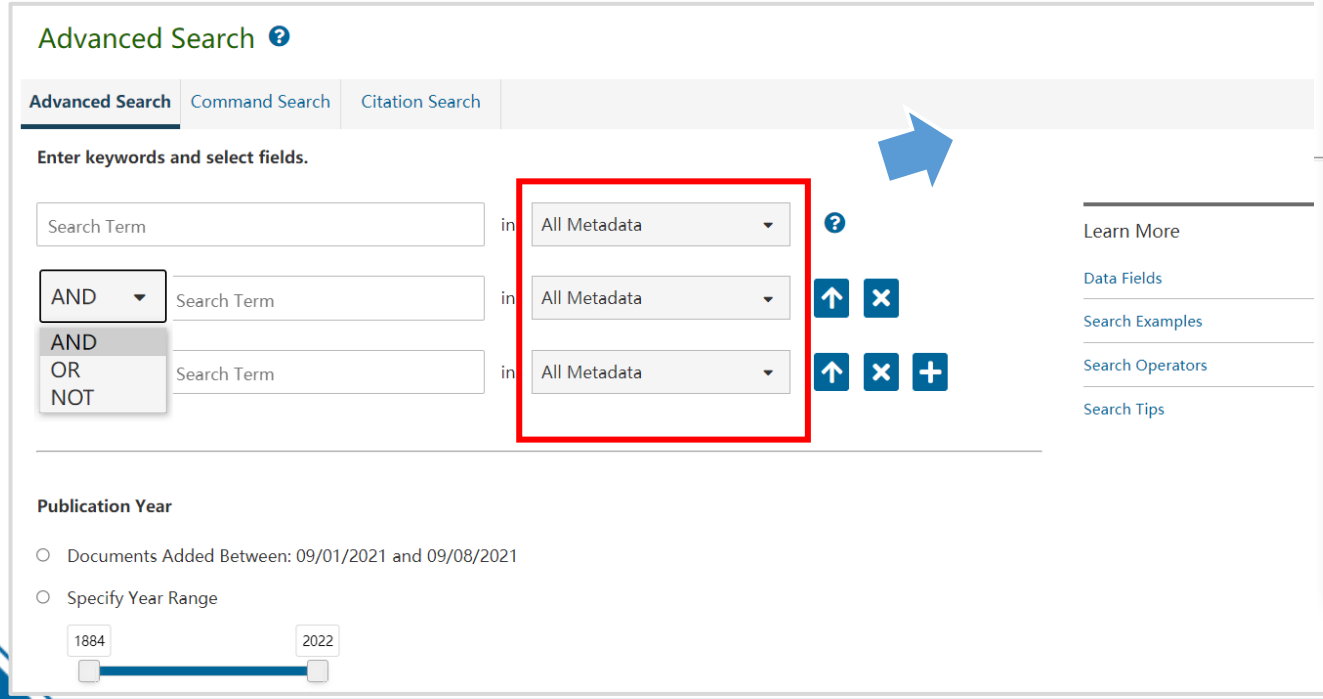

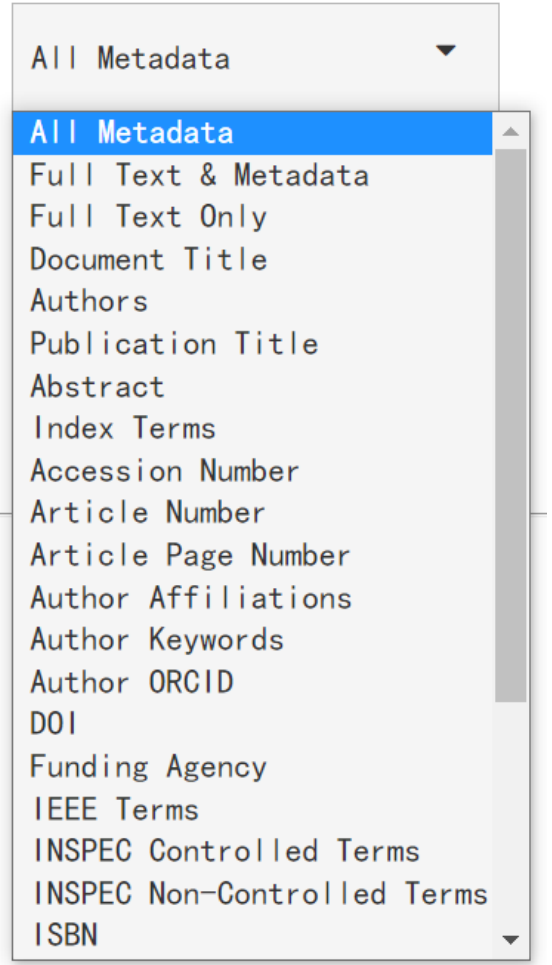

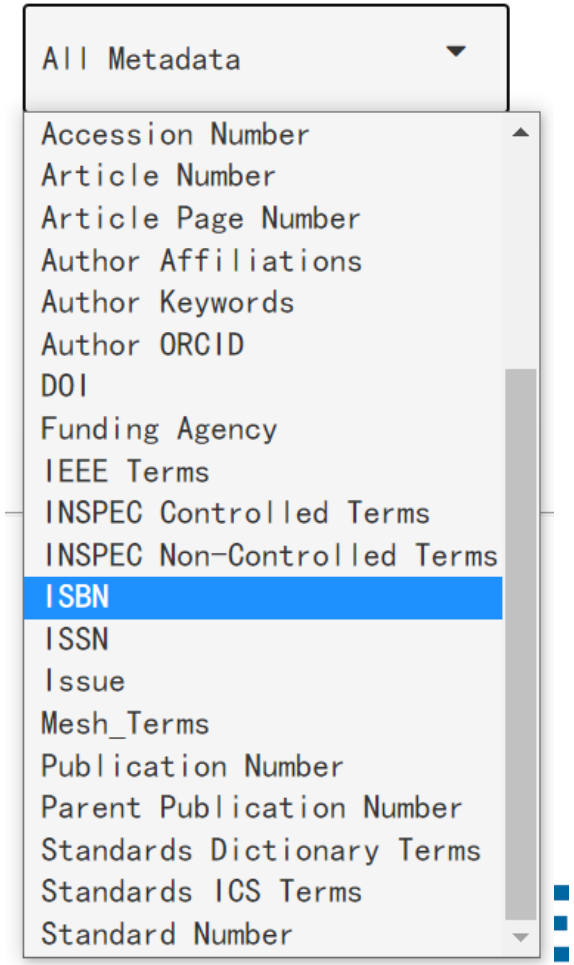

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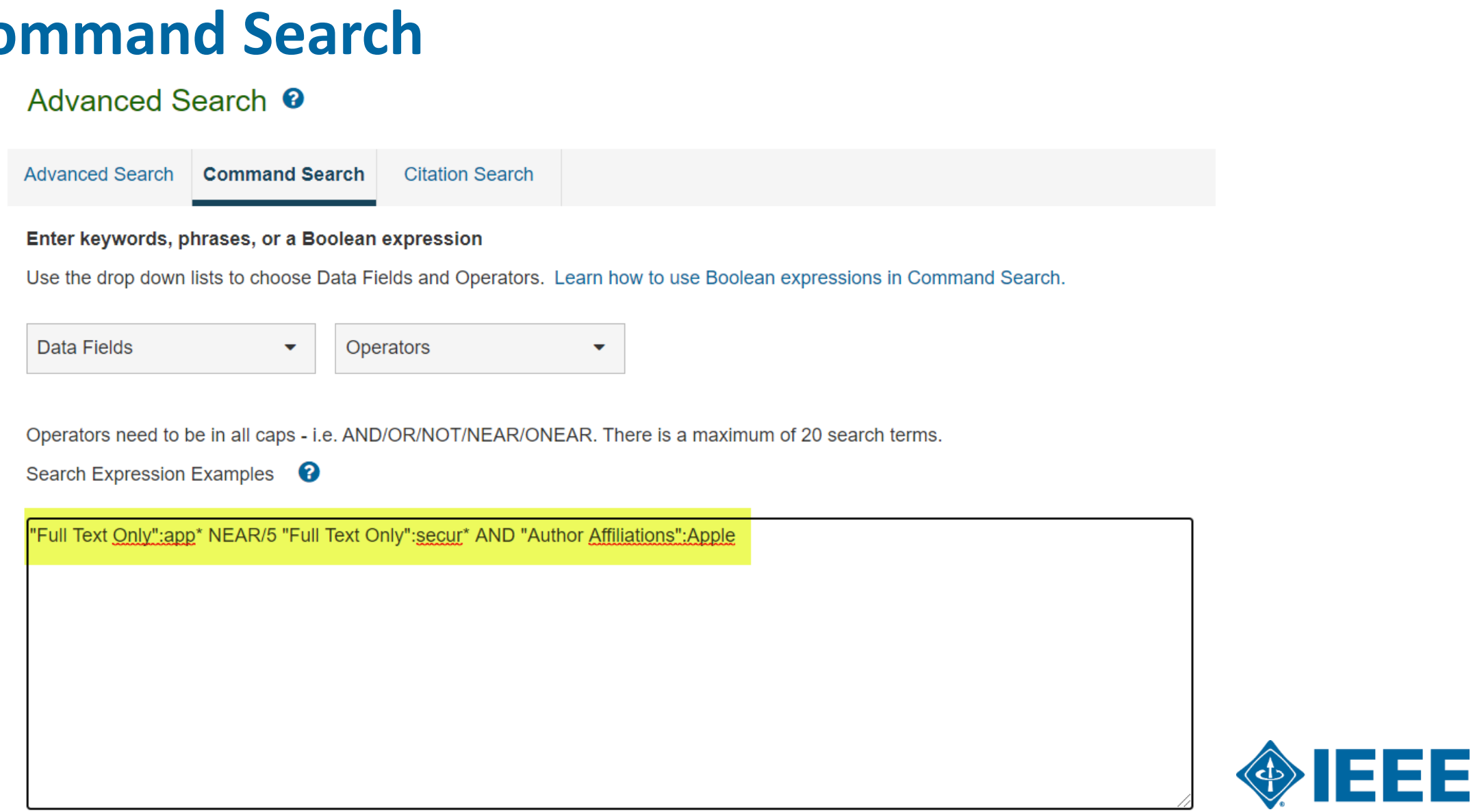

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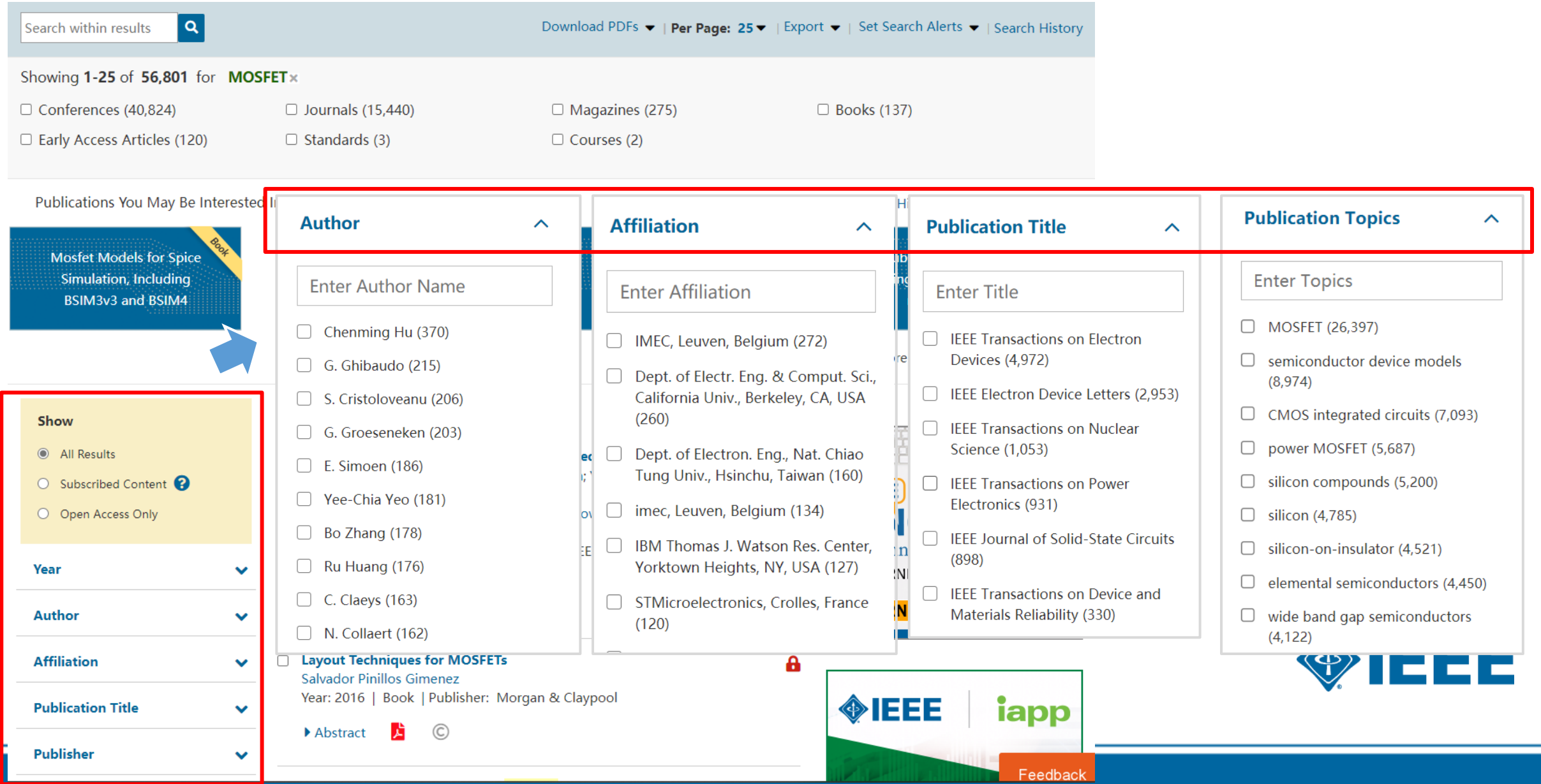

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T. Tang; C. Burkhart

IEEE Transactions on Dielectrics and Electrical Insulation

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Abstract:
The ultra-fast switching of power MOSFETs, in about 1 ns, is very challenging. This is largely due to the parasitic inductance that is intrinsic to commercial packages used for both MOSFETs and drivers. Parasitic gate and source inductance not only limit the voltage rise time on the MOSFET internal gate structure but can also cause the gate voltage to oscillate. This paper describes a hybrid approach that substantially reduces the parasitic inductance between the driver and MOSFET gate, as well as between the MOSFET source and its external connection. A flip-chip assembly is used to directly attach a die-form power MOSFET and driver on a PCB. The parasitic inductances are significantly reduced by eliminating bond wires and minimizing lead length. The experimental results demonstrate ultra-fast switching of the power MOSFET with excellent control of the gate-source voltage.

Published in: IEEE Transactions on Dielectrics and Electrical Insulation (Volume: 16 , Issue: 4, August 2009)

Page(s): 967 - 970

INSPEC Accession Number: 10847239

Date of Publication: 28 August 2009

DOI: 10.1109/TDEI.2009.5211841

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Power MOSFETs have great potential as switches for high speed high voltage applications like pulsed power. the theoretical carrier transit time from drain to source is on the order of 200 ps in any cell of the silicon die [1]. Although the power MOSFET is

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Quantitative Discussion on Sensitivity to Terahertz Waves of Detectors Made of MOSFET and High-Electron Mobility Transistor
2019 7th International Japan-Africa Conference on Electronics, Communications, and Computations

References

Citation Map

1. R. Mitova and R. Ghosh, "Investigations of 600V GaN HEMT and GaN diode for the power converter applications", *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2441-2452, May 2014.
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2. "Application Advantages and Disadvantages of Modern Fast Switching MOSFETs in VRM", *PCIM Europe*, 2016.
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3. Christian R. Müller and Stefan Buschhorn, "Impact of module parasitics on the performance of fast switching devices", *PCIM Europe*, 2014.
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4. Alan Elbanhawy, MOSFET Susceptibility to Cross Conduction, Power Electronics Technology, April 2005.
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5. Alan Elbanhawy, AN-7019 Limiting Cross-Conduction Current in Synchronous Buck Converter Designs, Fairchild Semiconductor.

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1. Masahiro Koyama, Kentaro Ikeda, Kazuto Takao, "Novel cascode GaN module integrated a single gate driver IC with high switching speed controllability", *Power Electronics and Applications (EPE'18 ECCE Europe) 2018 20th European Conference on*, pp. P.1-P.8, 2018.
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2. Tianhua Zhu, Fang Zhuo, Feng Wang, Hailin Wang, Xiaoping Sun, Shuhuai Shi, Baohui Ma, "Quantitative Analysis and Suppression Strategies of Dv/dt Induced Turn-on of Cascode GaN FETs in Half-bridge Circuits", *Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia) 2018 1st Workshop on*, pp. 130-134, 2018.
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3. Tianhua Zhu, Fang Zhuo, Fangzhou Zhao, Feng Wang, Tong Zhao, "Quantitative Model-Based False Turn-on Evaluation and Suppression for Cascode GaN Devices in Half-Bridge Applications", *Power Electronics IEEE Transactions on*, vol. 34, no. 10, pp. 10166-10179, 2019.
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Chenming Hu

Department of Electrical Engineering and Computer Science, University of California, Berkeley, Berkeley, CA, USA

Chenming Hu (F' 03) is the TSMC Distinguished Professor Emeritus of University of California Berkeley, Berkeley, CA, USA. He is a Former Chief Technology Officer of TSMC. He is a Board Director of SanDisk Inc., and of the non-profit Friends of Children with Special Needs. He is well known for his work on the 3-D transistor, FinFET, which can be scaled to single digit nanometers. He has developed widely used IC reliability models and led the research of BSIM—the first industry—standard SPICE model used by most IC companies to design CMOS products since 1996. He was a recipient of the IEEE Andrew Grove Award, the Solid State Circuits Award and Nishizawa Medal, the Kaufman Award of the EDA industry, the University Research Award of the U.S. Semiconductor Industry Association, and the UC Berkeley's Highest Honor for teaching—the Berkeley Distinguished Teaching Award.

SECTION I.

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Biography
Chenming Hu (F' 90) received the Ph.D. degree in electrical engineering from the University of California (UC) at Berkeley, Berkeley, CA, USA. He is TSMC Distinguished Professor Emeritus with UC Berkeley. He is the 2020 IEEE Medal of Honor recipient and has received the US National Medal of Technology and Innovation from President Obama in 2016 for developing transistor compact models BISM, first 3D transistor FinFET, and semiconductor reliability physics.

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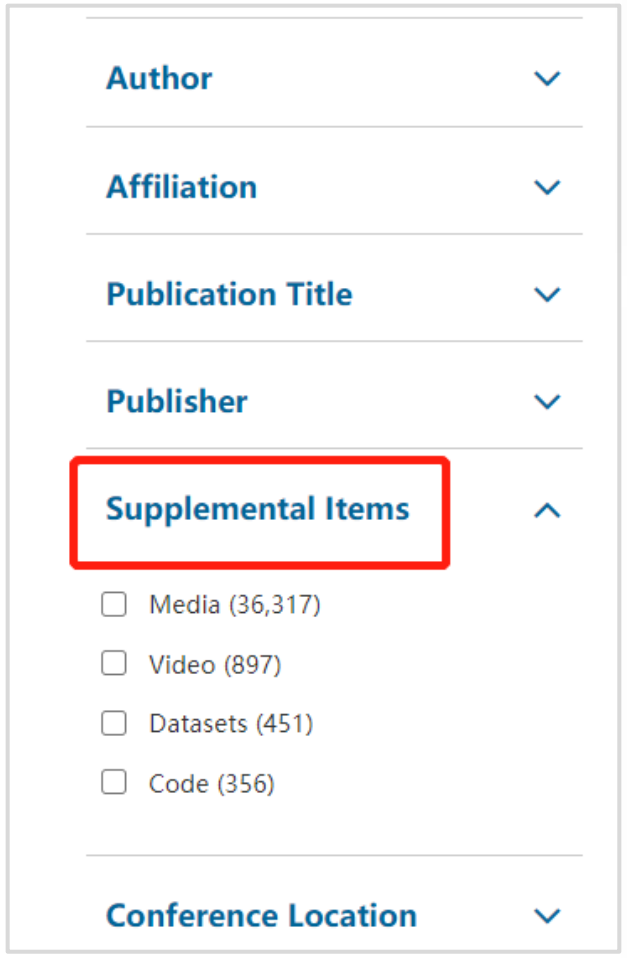

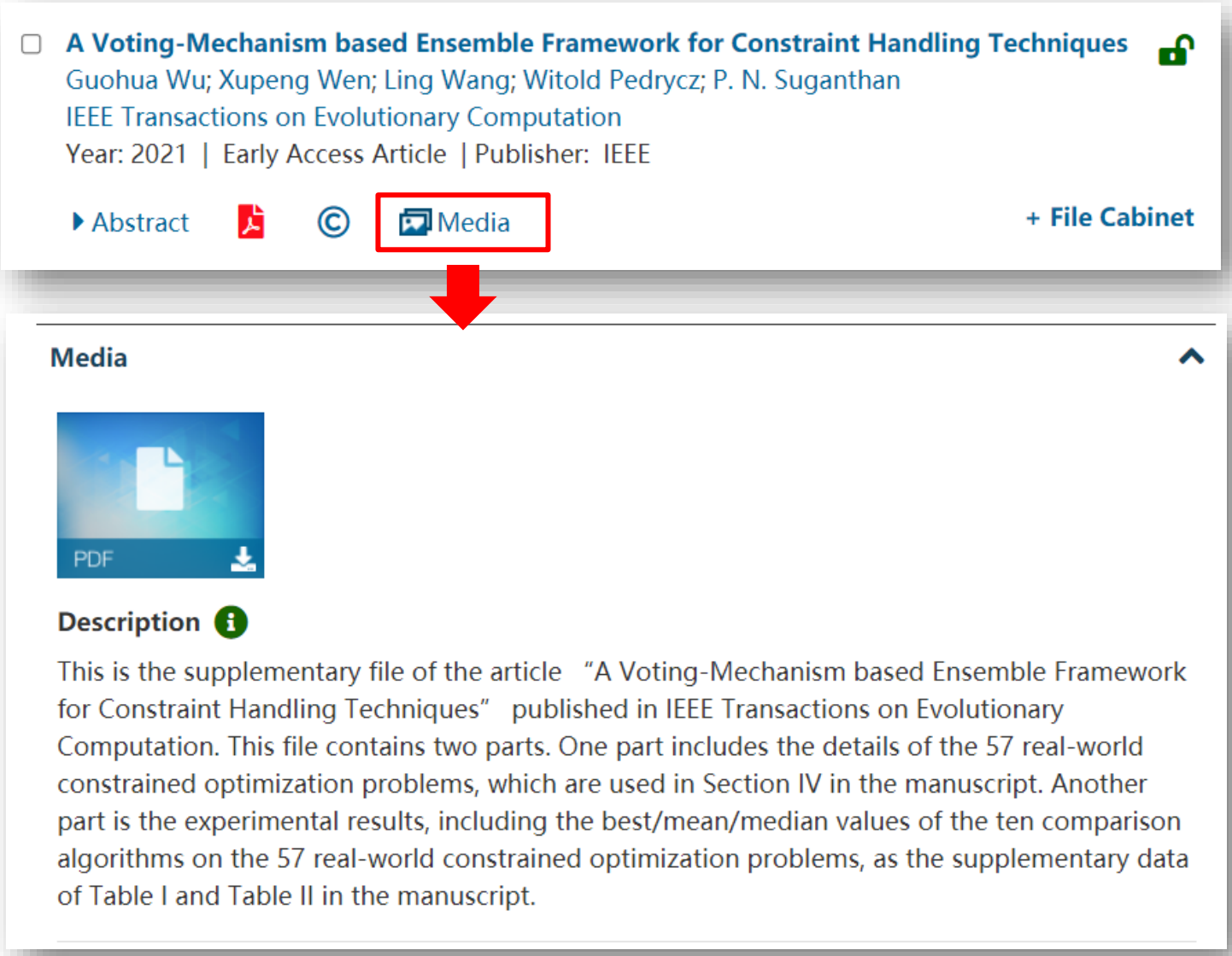

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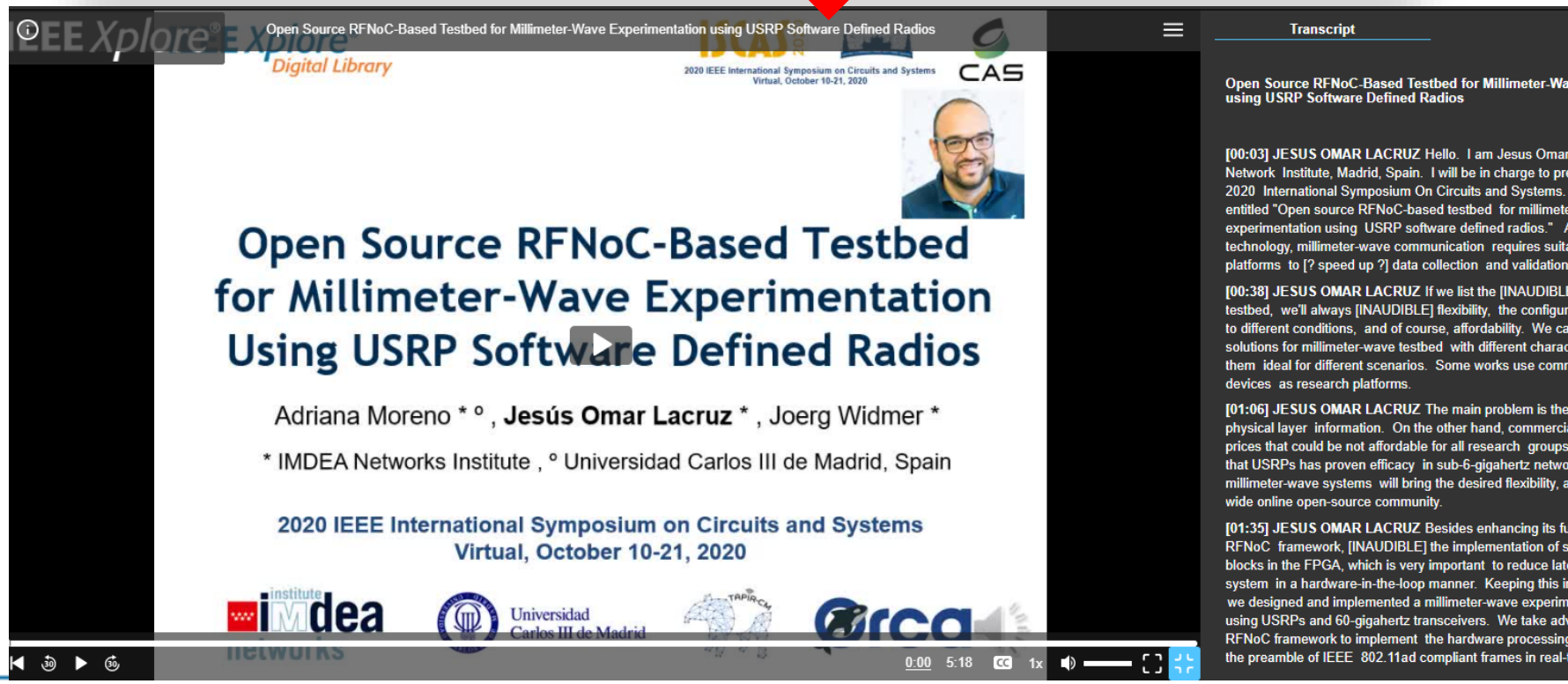

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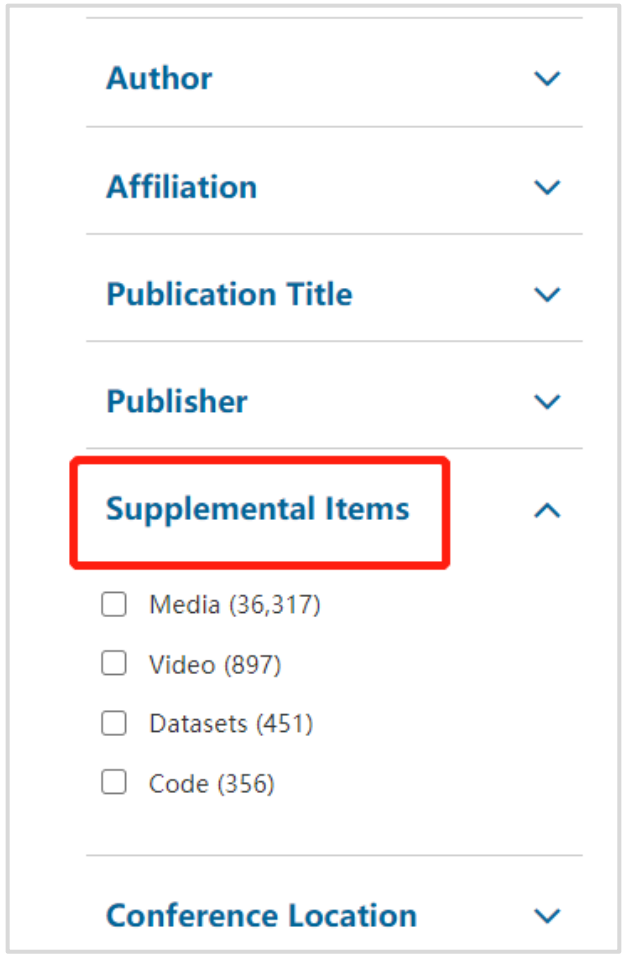

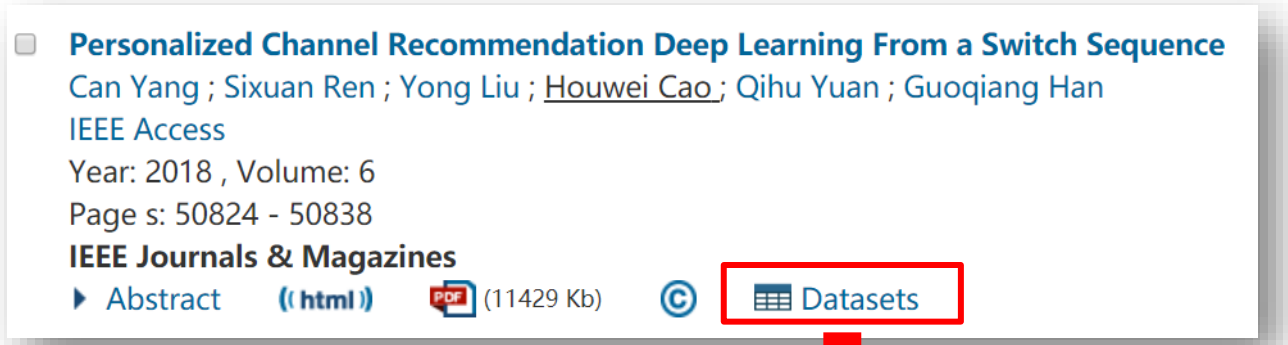

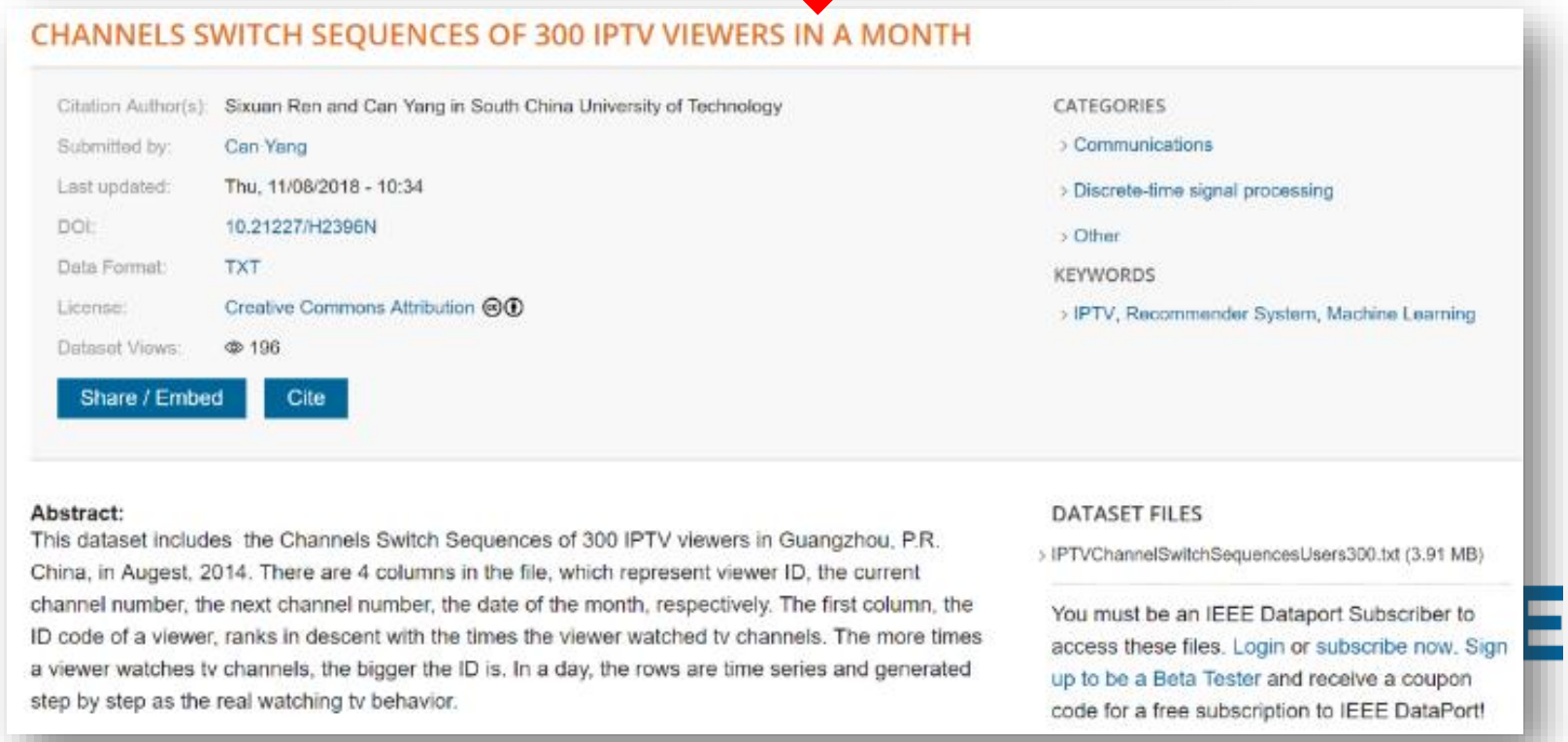

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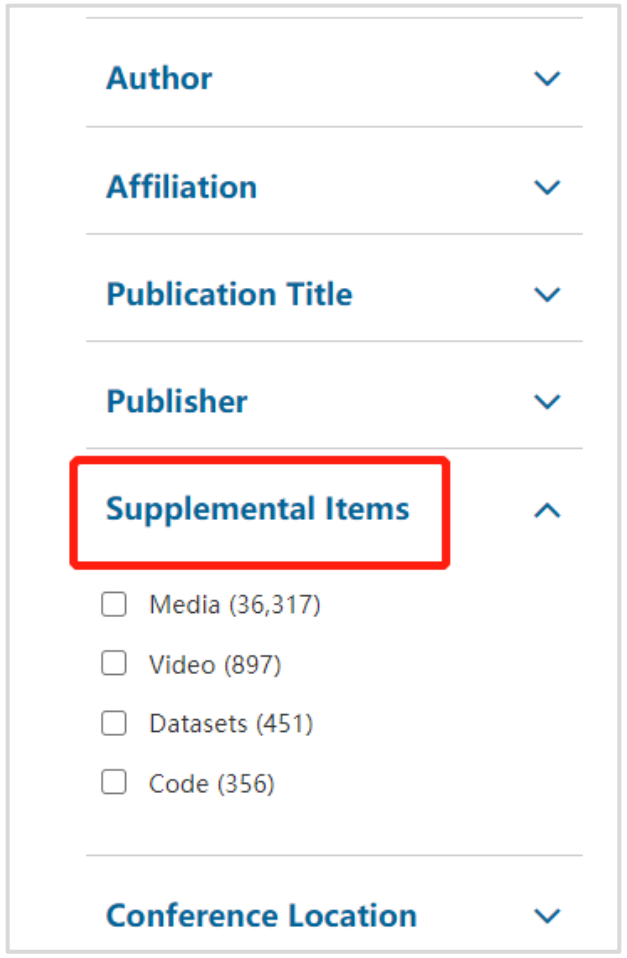

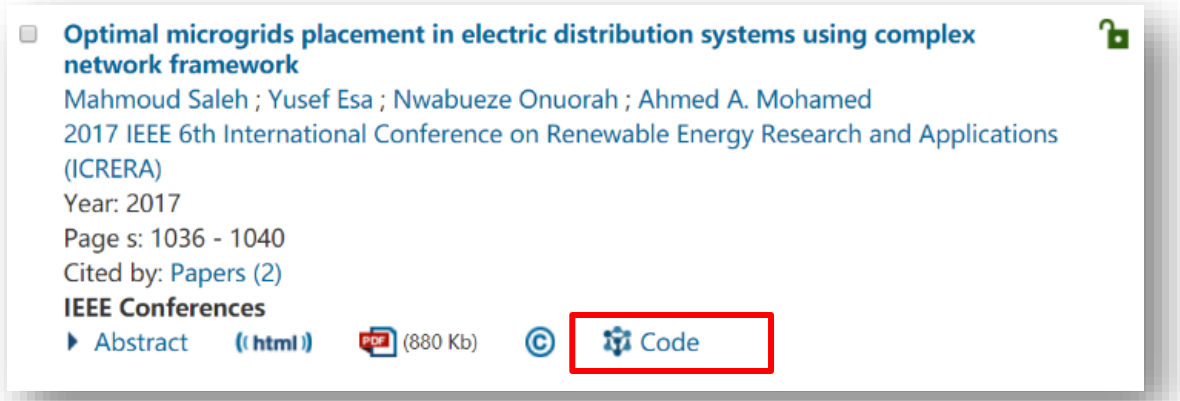

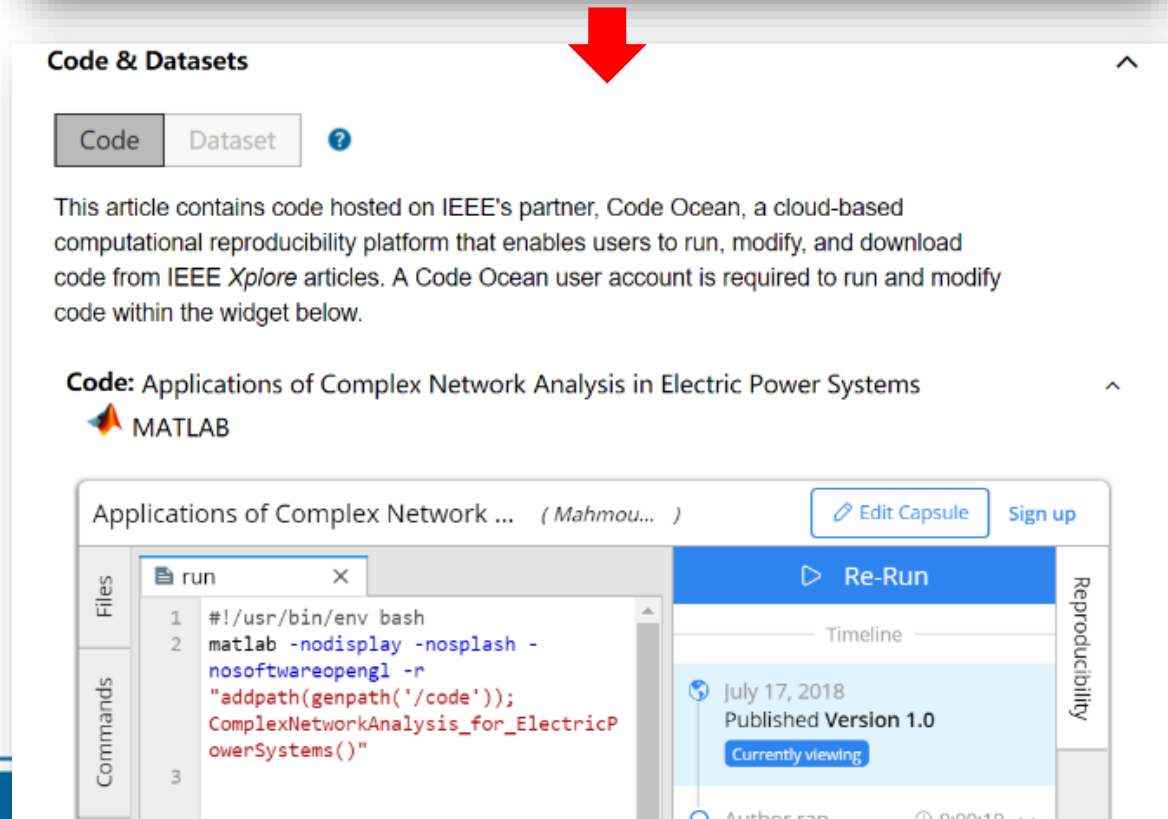

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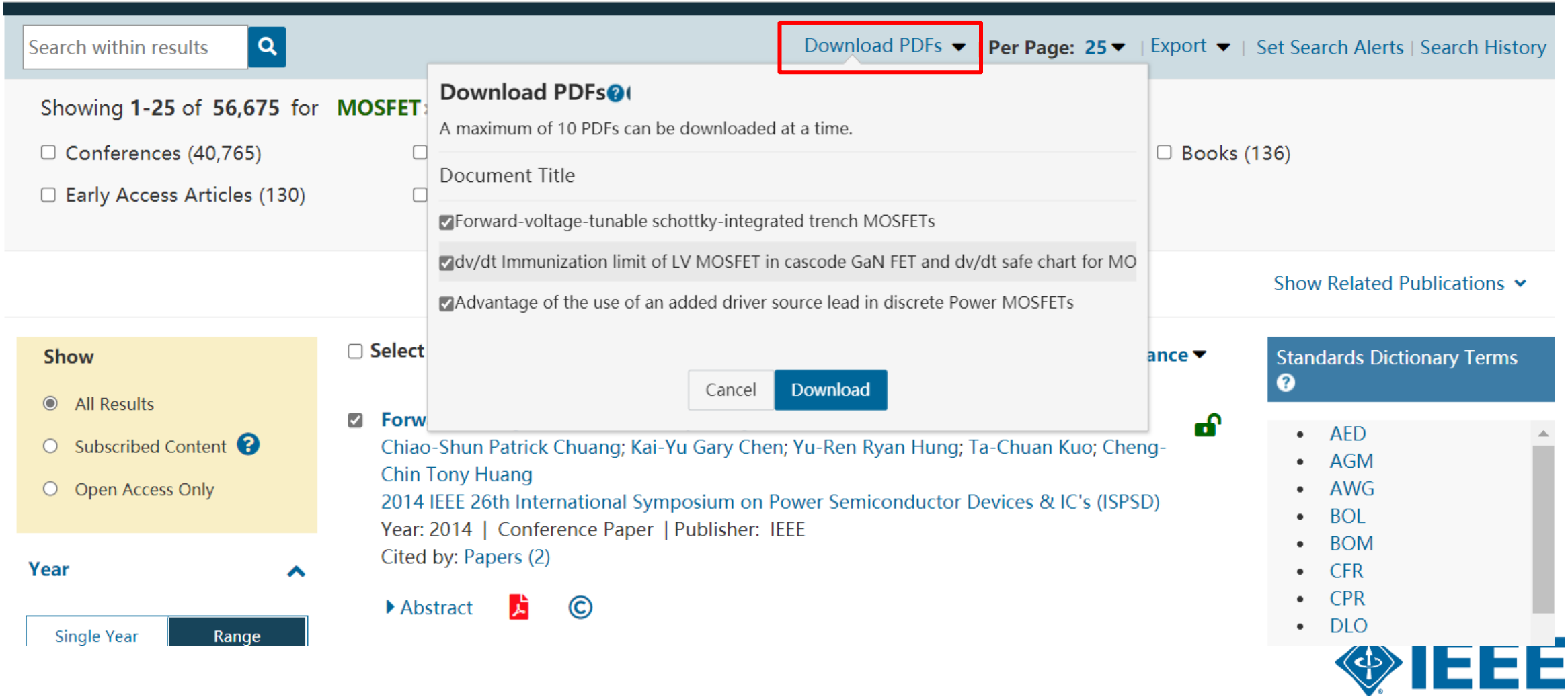

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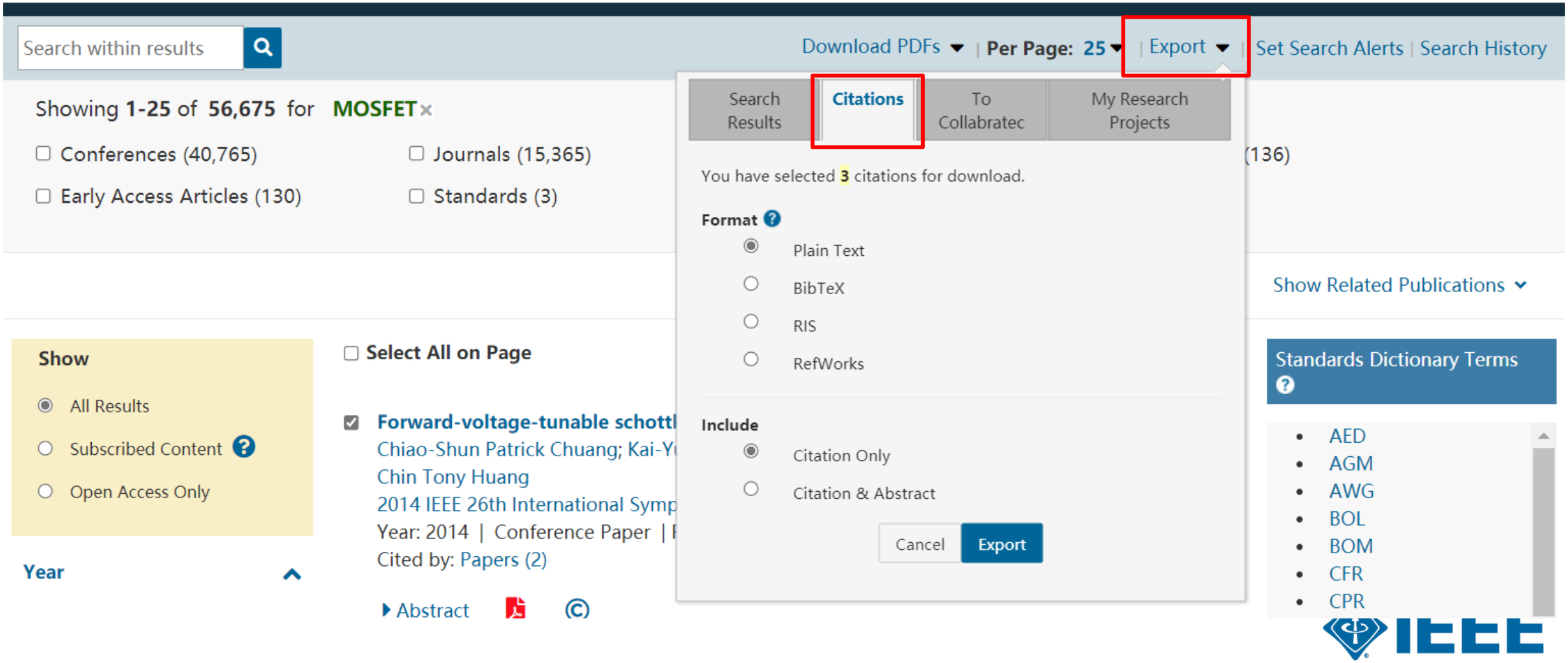

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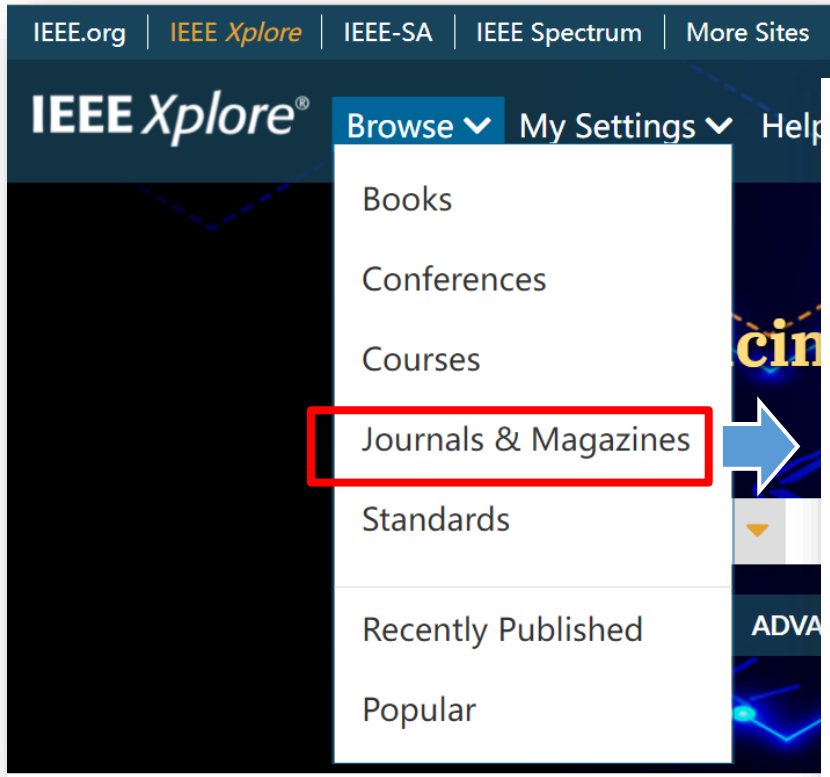

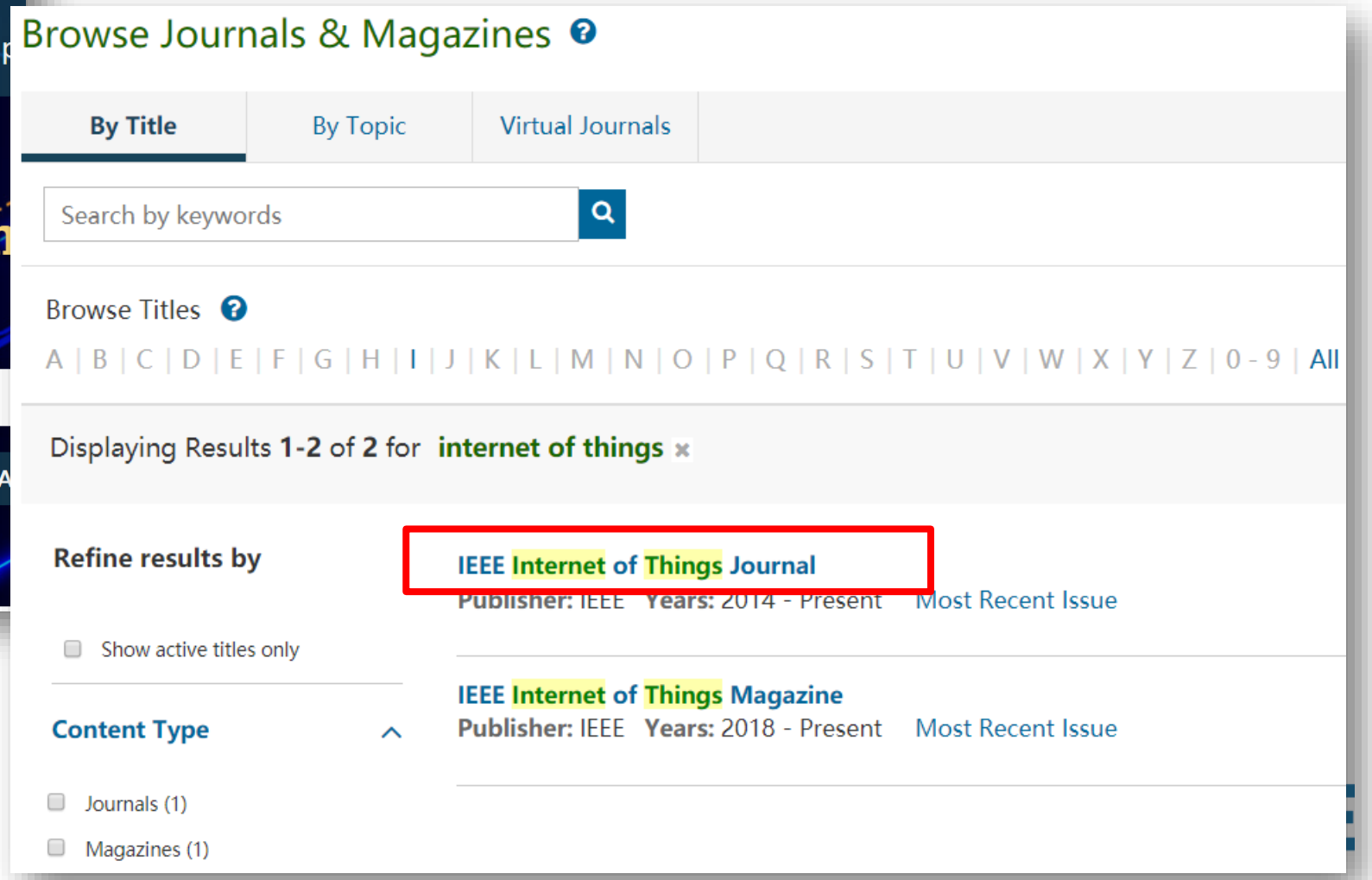

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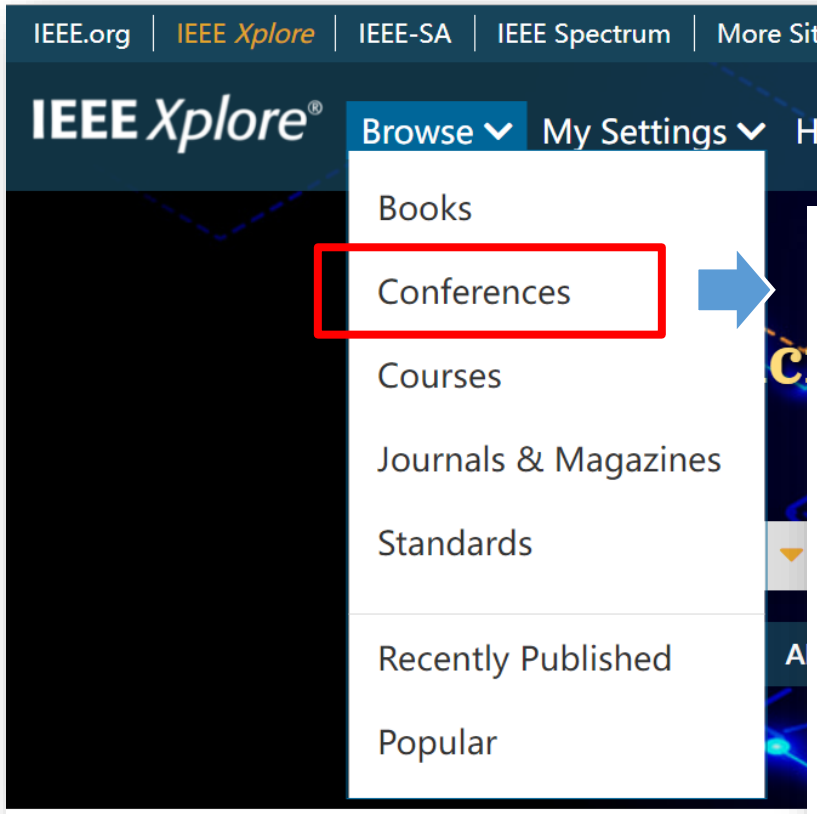

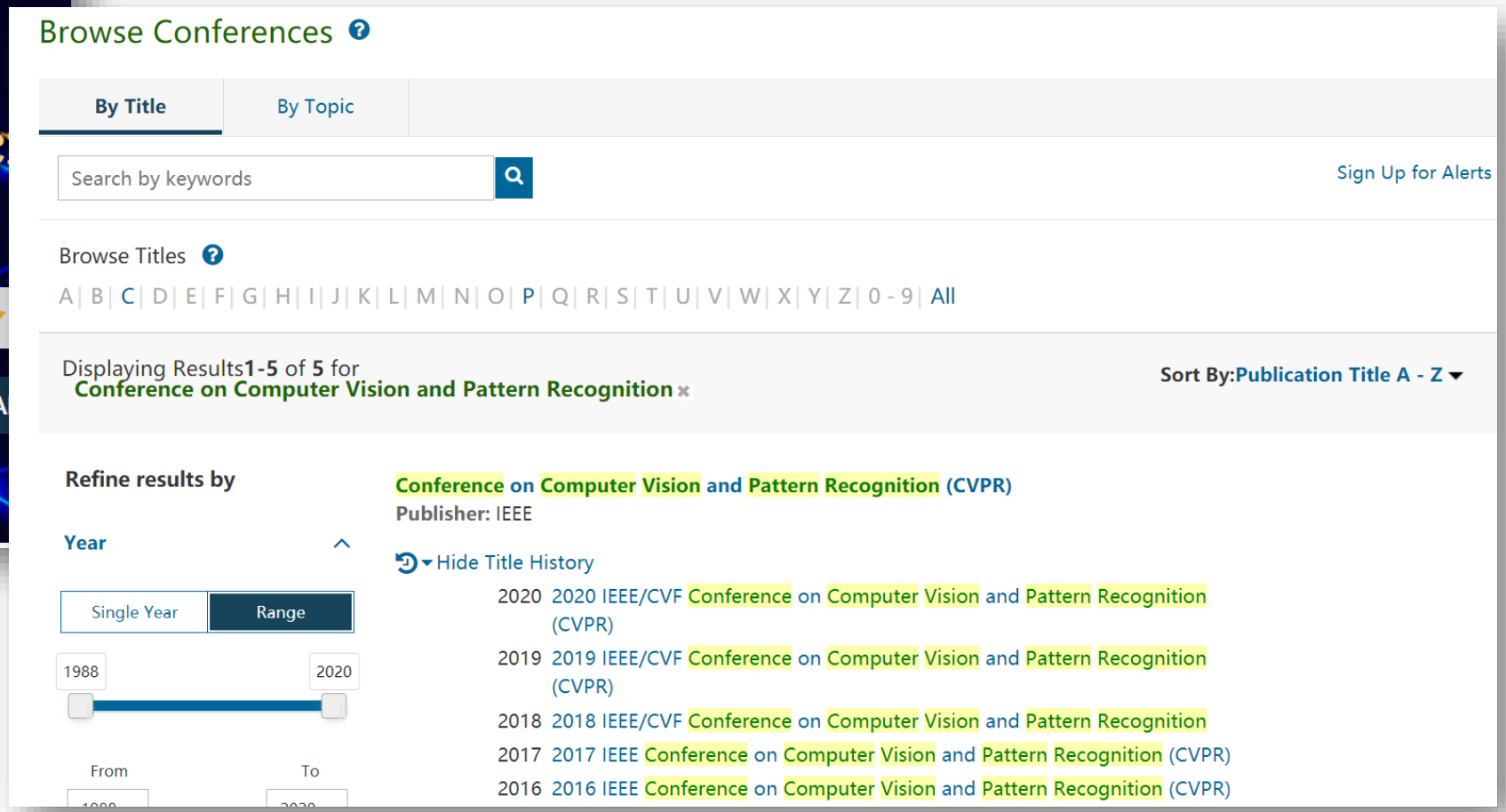

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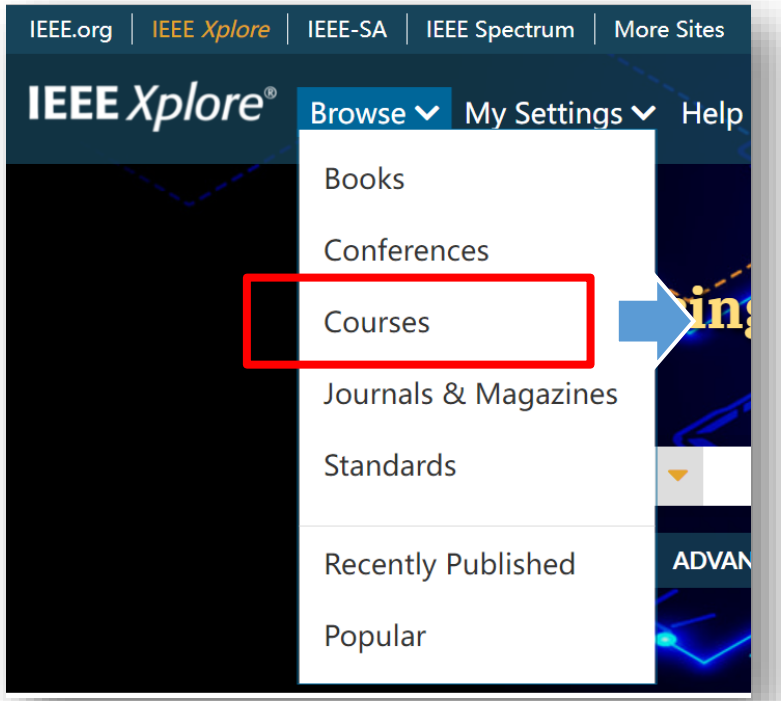

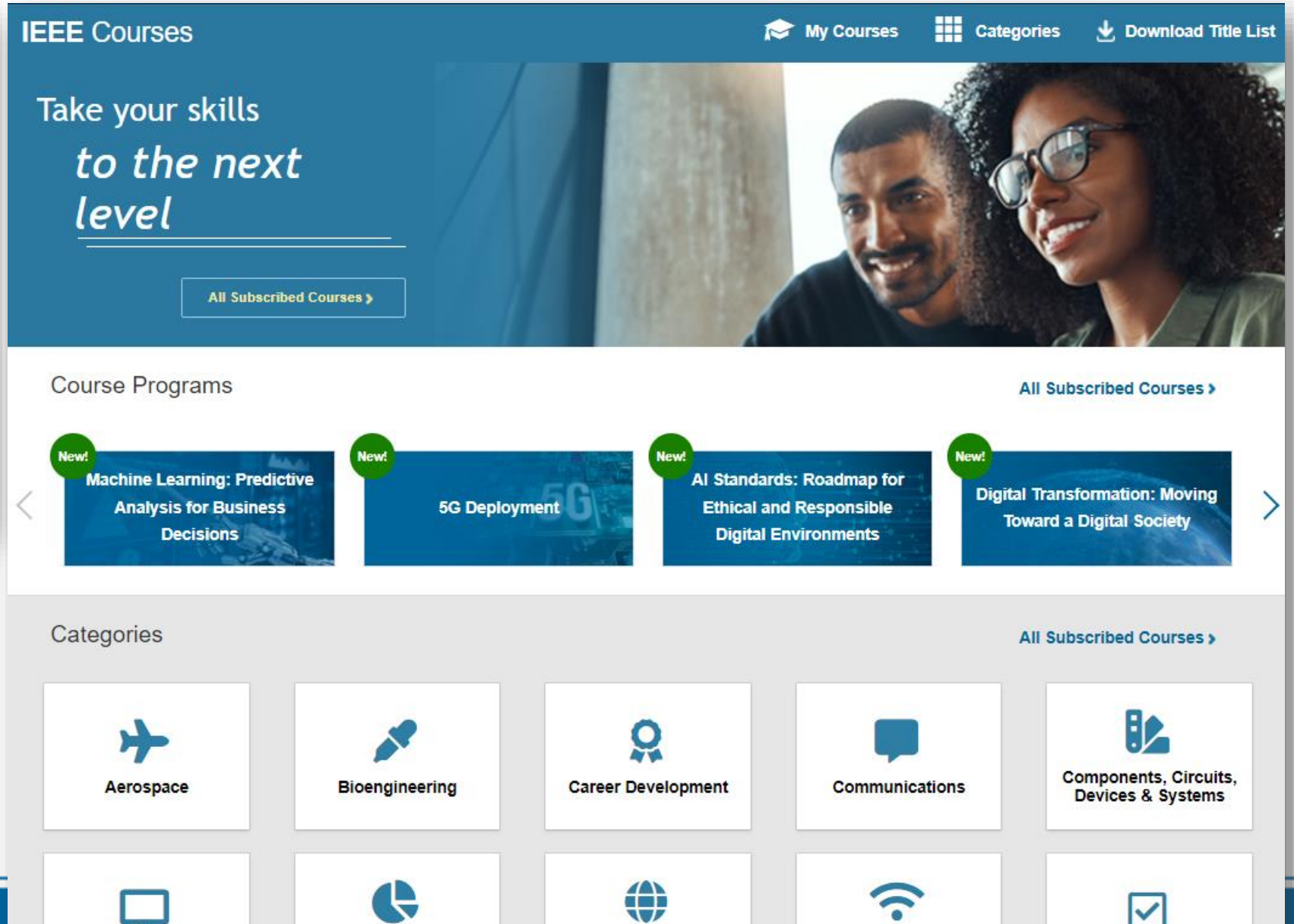

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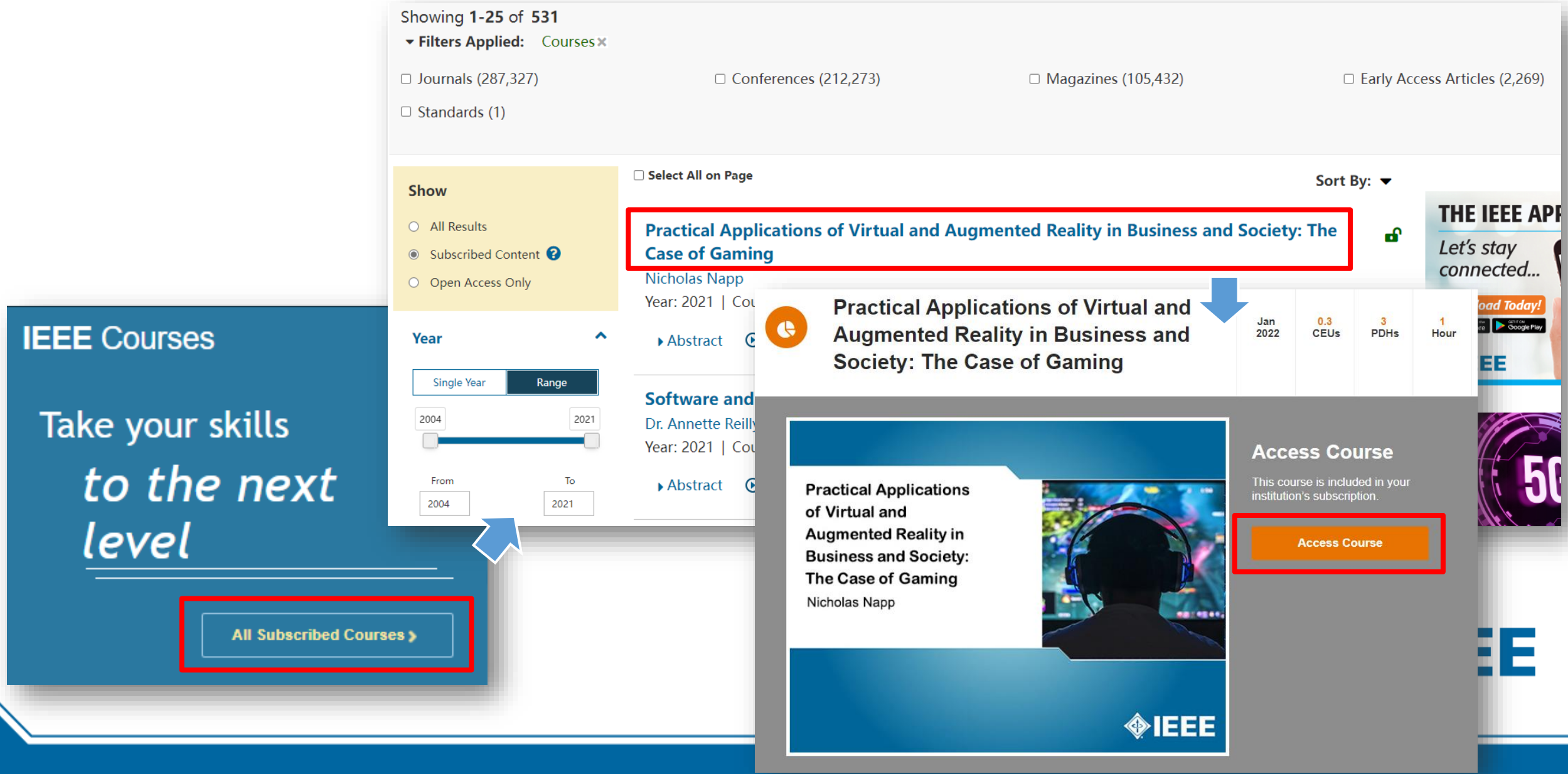

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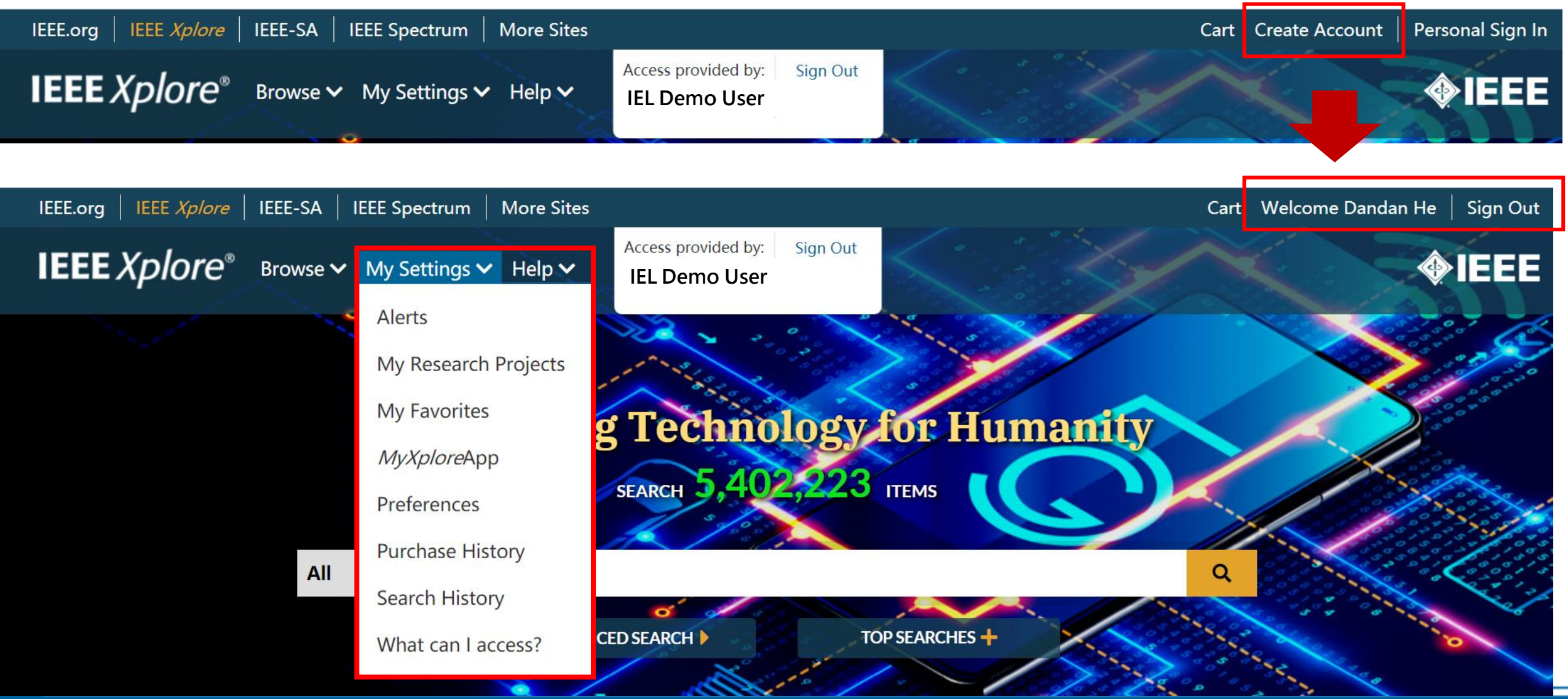

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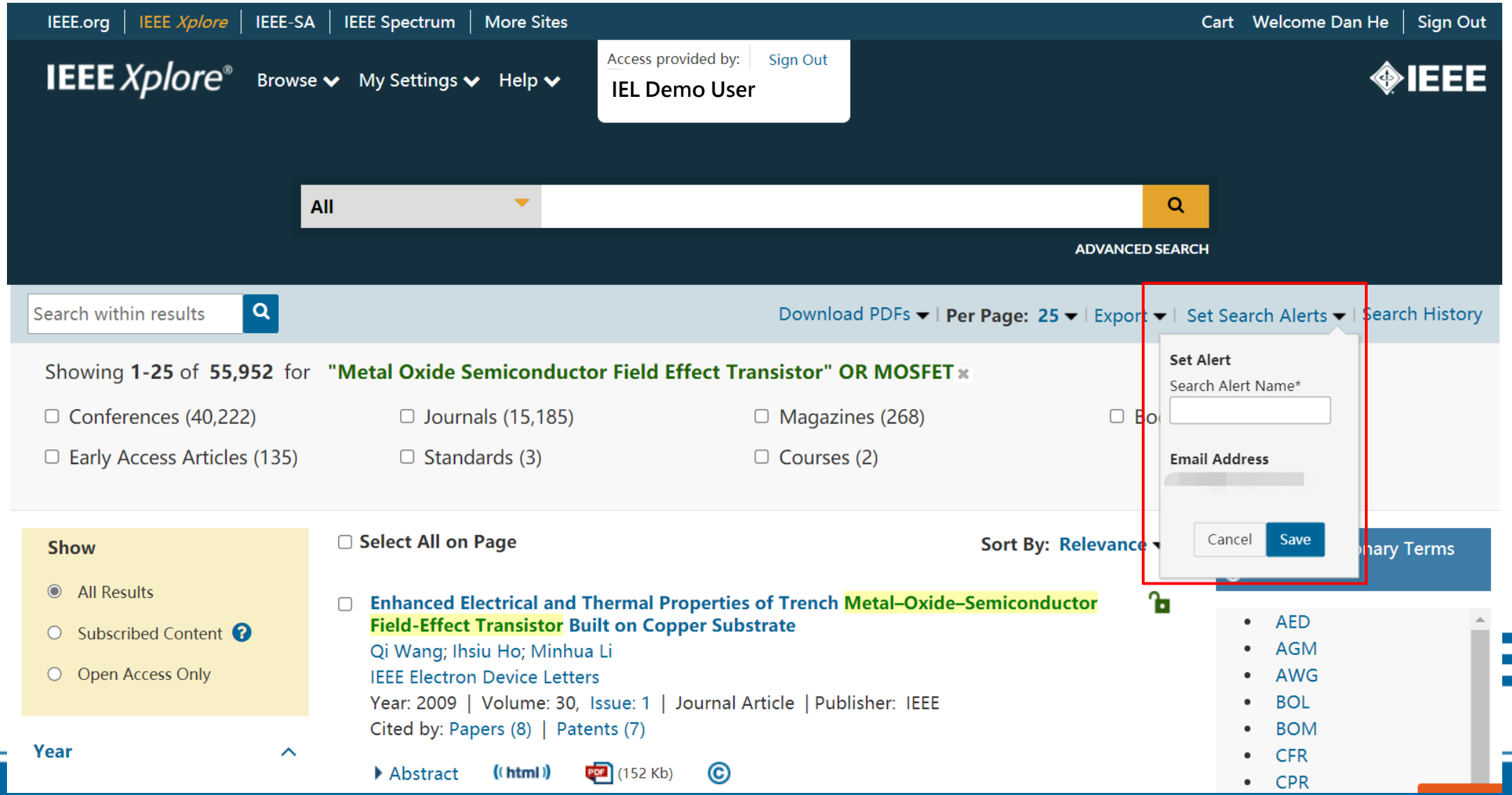

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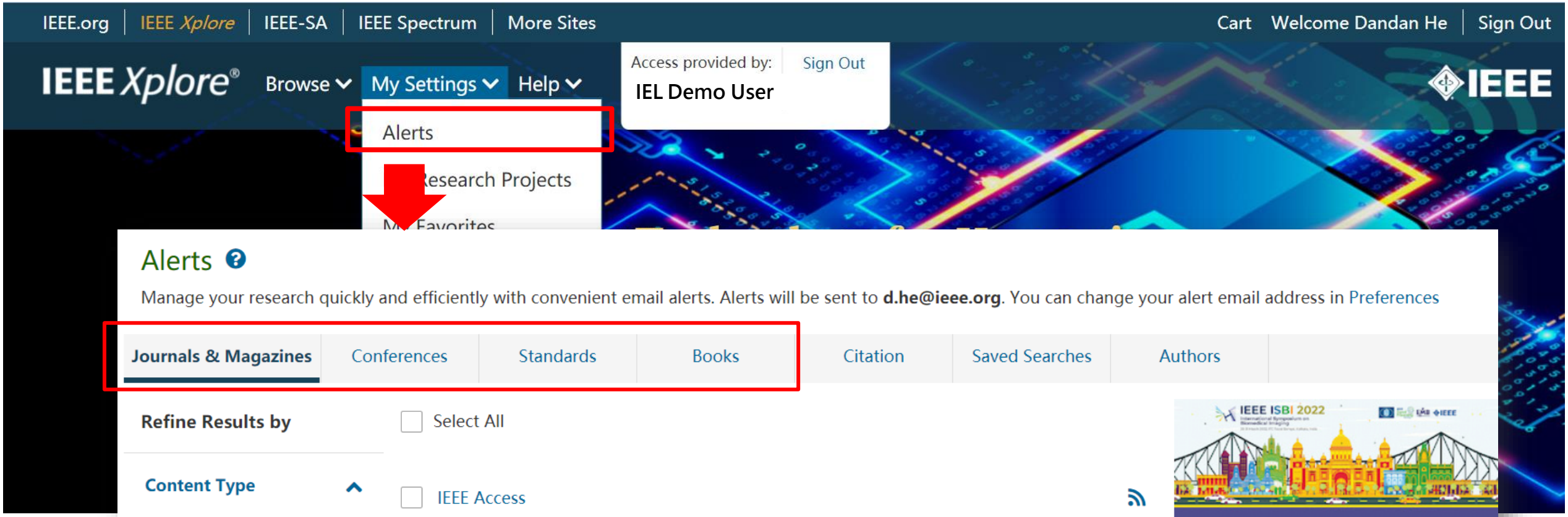

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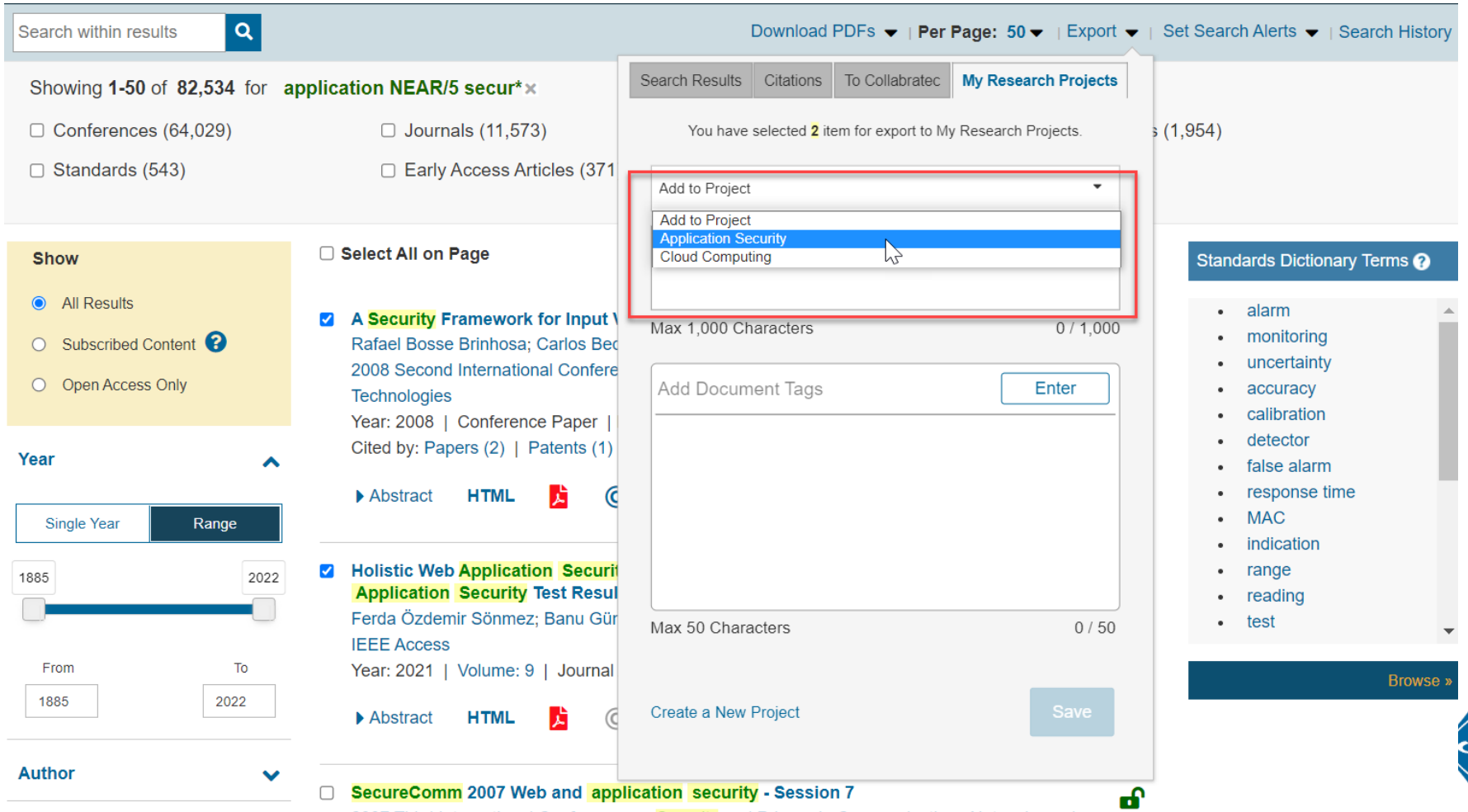

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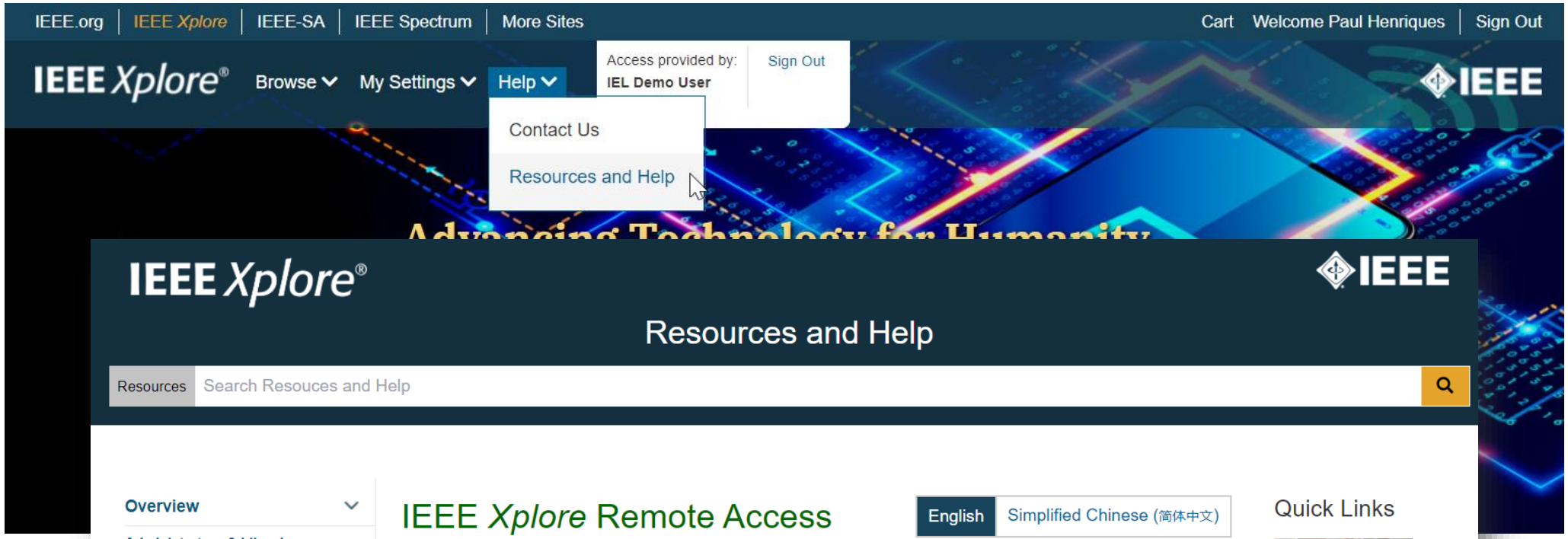

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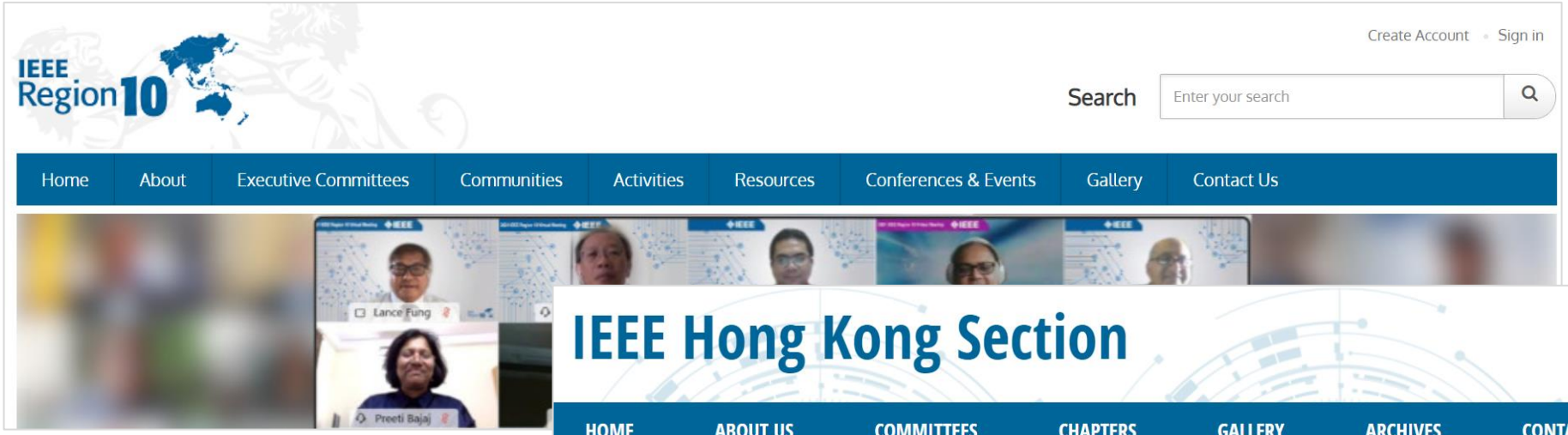

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